C 3006

OPERATING MANUAL

MODEL 5110
FREQUENCY SYNTHESIZER

WAVETEK®

OPERATING MANUAL

MODEL 5110
FREQUENCY SYNTHESIZER

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SPECIFICATIONS

OUTPUT SIGNAL

FREQUENCY RANGE:	DC to 2 MHz
FREQUENCY RESOLUTION:	0.001 Hz throughout entire range
OUTPUT IMPEDANCE:	50 ohms
AMPLITUDE:	1 VRMS, no load
OPTION 04:	10 V P-P, no load
ATTENUATOR - OPTION 02:	Provides from 0 to 85 db attenuation in steps of 1 db.

OUTPUT SIGNAL	DC	100KHz	500KHz	2 MHz
RMS FRACTIONAL DEVIATION 10 msec averaging 1 sec averaging	5×10^{-7} 5×10^{-9}			
PHASE NOISE In 30 KHz band excluding 1 Hz centered on carrier	-50 db			
SPURIOUS COMPONENTS	-70 db	-60 db	-50 db	
HARMONIC COMPONENTS At 1 volt RMS output At 10 volts P-P output (Option 04)	-55 db -55 db	-50 db -50 db	-45 db -40 db	
FREQUENCY RESPONSE (full output) No load 50 ohm load	±.25 db ±.25 db		±.5 db +.5, -2.5 db	
ATTENUATOR RESPONSE (Option 02)	±.5 db to 60 db		See Figure 2.7	

PROGRAMMING

FREQUENCY SELECTION:	31 bits in BINARY or 37 bits in BCD format. Format selected by one control bit.
ATTENUATION SELECTION: (Option 02)	7 bits (40, 20, 10, 8, 4, 2, 1 db).
LOADING SEQUENCE:	Synchronous loading of all frequency and attenuation bits in one parallel word, or in four 12- bit bytes. Sequence selected by one control bit.
PROGRAMMING DELAY:	1.5 usec for BINARY-WORD with phase and amplitude continuity maintained. 20 usec for BCD-WORD with output reset to zero phase during delay. 20 usec minimum for four BCD or BINARY bytes with output reset to zero phase during programming.
UPDATE RATE:	625 nsec for BINARY-WORD mode. 18 usec for BCD-WORD and BYTE modes.
ZERO PHASE RESET:	Output signal may be asynchronously reset to zero phase via one control bit. There is a delay of approximately 800 nsec to the output. This line may also be used as a load acknowledge output.

ELECTRICAL AND PHYSICAL

OPERATING TEMPERATURE:	0°C to +50°C ambient.
STORAGE TEMPERATURE:	-20°C to +70°C.
POWER REQUIREMENTS:	115 or 230 volts AC, ±10% 50-60 Hz, 65 watts.
SIZE:	3-1/2"H x 17"W x 13"D
WEIGHT:	21 lbs. Shipping weight 25 lbs.
ACCESSORIES SUPPLIED:	Programming connector and instruction manual.

INTERNAL CRYSTAL REFERENCE

TEMPERATURE STABILITY:	
OPTION 01:	$\pm 1 \times 10^{-8}$ over 0°C to 55°C range *
OPTION 06:	$\pm 1 \times 10^{-6}$ over 0°C to 55°C range
AGING RATE:	
OPTION 01:	1 part in 10^9 per day. *
OPTION 06:	1 part in 10^8 per day; 1 part in 10^6 per year.
EXTERNAL 1 MHz REFERENCE:	Accepts external 1 MHz reference to phase lock internal crystal (Option 01 or 06).
EXTERNAL 8 MHz REFERENCE:	Required for units with no internal crystal, but also may be used with Option 01 or 06, bypassing internal crystal.
EXTERNAL REFERENCE SIGNAL:	TTL levels with one standard TTL load. Schmitt-trigger conditioned. Will also accept bipolar signals up to ±5 volts peak.

REFERENCE OUTPUT

FREQUENCY:	8 MHz or 1 MHz (selectable internally) derived from the internal crystal reference, or 1 MHz only derived from an external 8 MHz reference.
WAVEFORM:	TTL, square wave for 1 MHz or pulse waveform for 8 MHz.
DRIVE CAPABILITY:	Up to 30 standard TTL loads. Rear panel BNC jack.

* The specifications for the Option -01 frequency standard apply after a warm-up stabilization period of 72 hours.

OPTIONS

OPTION 01:	HIGH STABILITY CRYSTAL REFERENCE (Proportional Oven Control)
TEMPERATURE STABILITY:	$\pm 1 \times 10^{-8}$ over 0°C to 55°C range
AGING RATE:	1 part in 10^9 per day.
STABILIZATION PERIOD:	72 hours
OPTION 02:	PROGRAMMABLE ATTENUATOR
RANGE:	0 to 85 db in 1 db steps.
PROGRAMMING DELAY:	Typically less than 5 msec.
OPTION 04:	10 V P-P OUTPUT AMPLITUDE (Instead of 1 VRMS) See signal specification chart.
OPTION 06:	TEMPERATURE COMPENSATED CRYSTAL REFERENCE
TEMPERATURE STABILITY:	$\pm 1 \times 10^{-6}$ over 0°C to 55°C range
AGING RATE:	1 part in 10^8 per day; 1 part in 10^6 per year.

SECTION 1 - INSTALLATION AND THEORY OF OPERATION

1.0 INSPECTION

This instrument was carefully inspected and tested prior to shipment. It was operated for at least 100 hours to reduce the probability of early failure. The instrument should be inspected for physical damage incurred in transit. When receiving a shipment from a carrier, inspect the shipping carton in the presence of the carrier. If rough handling is evident take exception on the delivery receipt before accepting the shipment.

If no carton damage is obvious, but physical damage is discovered when the carton is opened, preserve the carton and packing materials, notify the carrier immediately and have them perform a written inspection of the carton and the contents.

It is recommended that conformance to specifications be verified upon receipt. In case of discrepancies, refer to the warranty in this manual.

1.1 POWER REQUIREMENTS

This instrument will operate from 115 vac (±10%) 50-60 Hz, or 230 vac (±10%) 50-60 Hz, selectable via a rear panel switch. The instrument is equipped with a three-wire power cable which connects the chassis to earth ground when plugged into a three-contact outlet. If a two-contact outlet is used in conjunction with a three-prong and two-prong adaptor, the pigtail of the adaptor should be connected to earth ground.

1.2 INSTALLATION

The chassis is designed to fit into a standard 19-inch equipment rack. Clearance of three inches must be provided at the rear of the unit for proper ventilation. Maximum ambient air temperature is 50°C or 122°F.

DATE	SYM	REVISION RECORD	AUTH	DR	CK

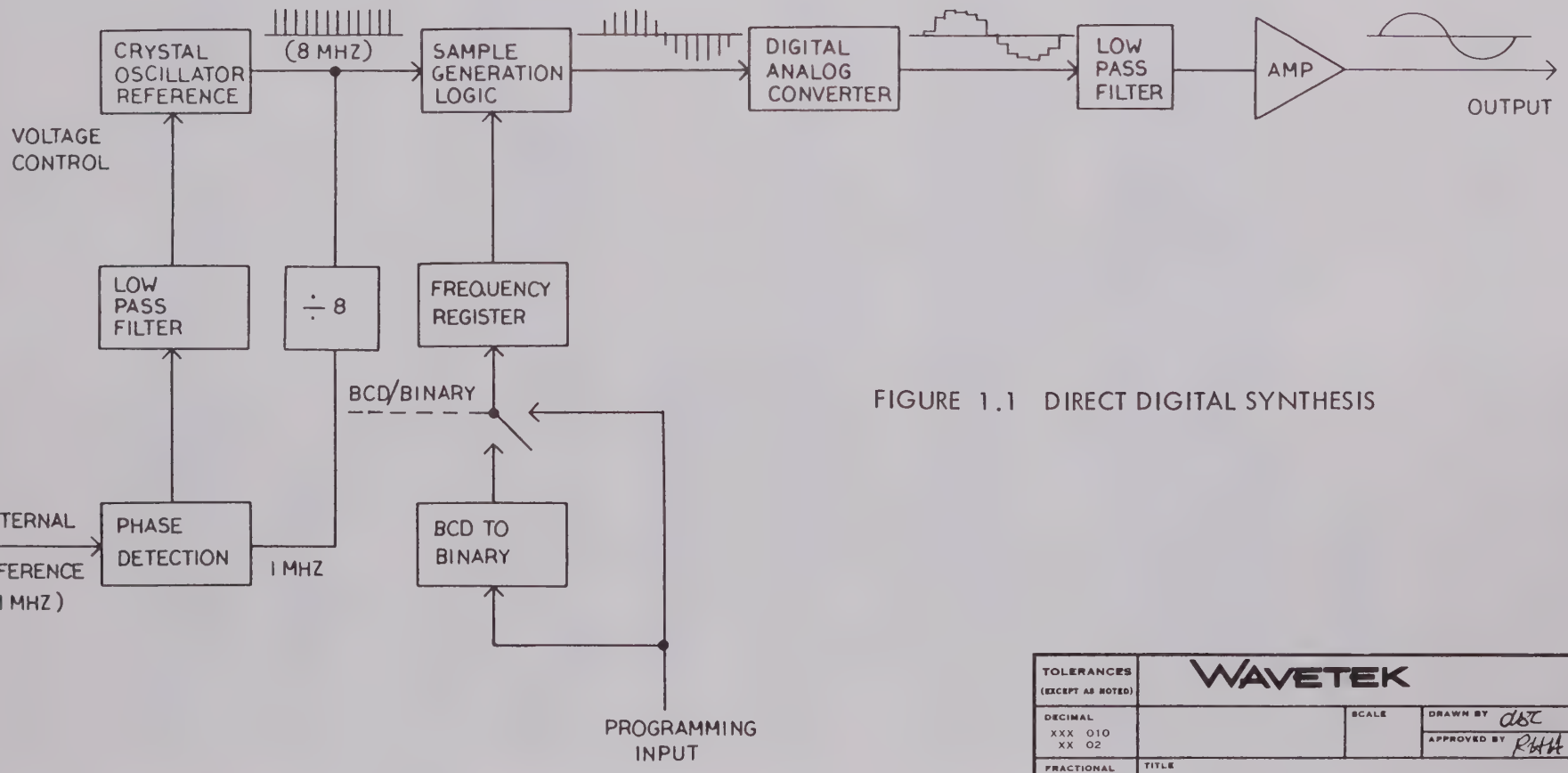


FIGURE 1.1 DIRECT DIGITAL SYNTHESIS

TOLERANCES (EXCEPT AS NOTED)	WAVETEK		
DECIMAL XXX 010 XX 02		SCALE	DRAWN BY dst
			APPROVED BY RHH
FRACTIONAL ± 1/64	TITLE DIRECT DIGITAL SYNTHESIS		
ANGULAR ±	DATE 2-28-72	DRAWING NUMBER	REV

R. S. KNAPP CO. INC. 52292

1.3 THEORY OF OPERATION

The Model 5110 utilizes direct digital synthesis techniques (Patent No. 3,735,269) to generate the output sinusoid. Samples of the sinusoid are digitally generated at an 8 MHz rate and are then converted to analog form by a Digital-to-Analog Converter (DAC) and a smoothing Low Pass Filter (LPF) cutting off at approximately 2.5 MHz. The amplitude of the digital samples is represented with 11 bits (including sign), and the phase accuracy of each sample is ±0.09°.

A block diagram of the unit is given in Figure 1.1. The stability of the 8 MHz system clock, whether supplied externally or from an internal crystal oscillator, directly determines the frequency stability of the output sinusoid. If an internal crystal is provided, it may be phase-locked to an external 1 MHz reference. Since excellent short-term stability is provided by the internal reference, the function of the external reference phase-locked loop is only to provide long-term stability, and hence, the loop bandwidth is fairly broad (~10 Hz).

The frequency value of the output sinusoid is stored in the Frequency Register in binary form with each 3-decade group (KHz, Hz, mHz) represented by a separate 10-bit binary number. A separate flip-flop stores the MHz bit. If the unit is programmed in this binary form, then no numerical conversion is required and the output frequency changes with no discontinuity in phase or amplitude. The delay from the programming inputs to the analog output in this mode is approximately 1.5 usec.

If the unit is programmed in BCD, then BCD-to-Binary conversion is required and the output is reset to zero phase during the conversion period. Programming in BCD or Binary can also be accomplished in four 12-bit bytes if the number of input lines is more important than the programming speed.

SECTION 2 - OPERATING PROCEDURES

2.0 OPERATING PROCEDURES

Figure 2.1 shows the front and rear panels of the instrument with controls and connectors identified in the key. The instrument is controlled exclusively by remote programming.

2.1 POWER SWITCH AND INDICATOR

The POWER SWITCH located on the front panel, switches AC line power to the unit. The green POWER INDICATOR verifies the presence of the 5-volt supply for the digital logic circuitry.

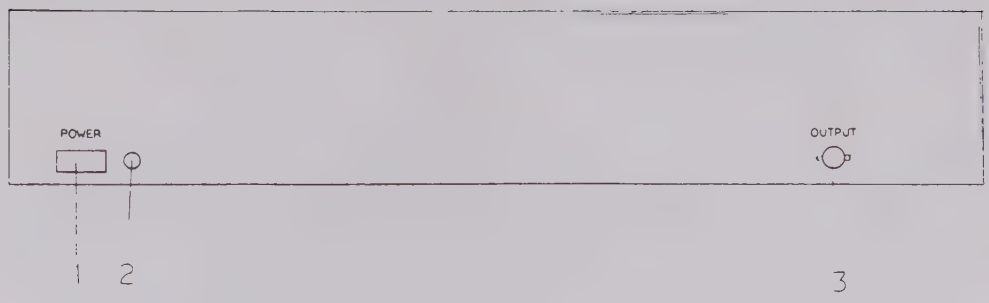
NOTE

For units equipped with the high-stability proportional-oven crystal (Option 01), power must be maintained (POWER INDICATOR ON) at least 72 hours prior to use, if full accuracy and drift performance of the crystal are to be realized.

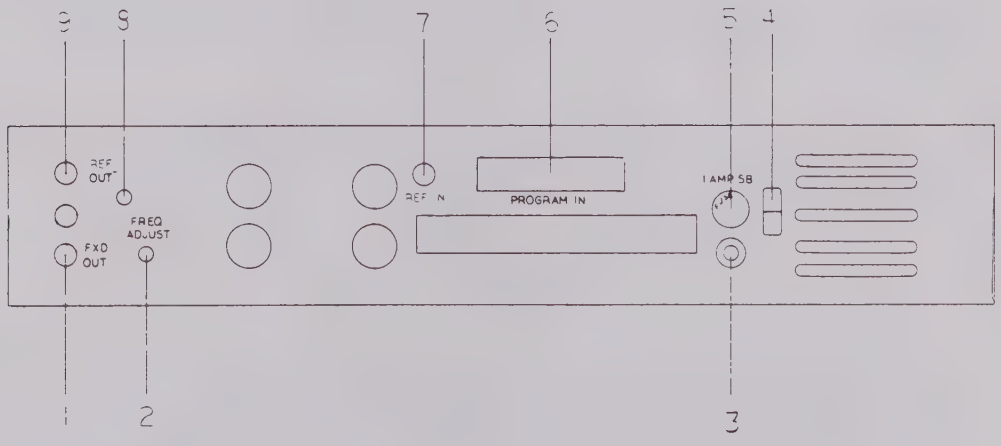
2.2 OUTPUT SIGNAL

The OUTPUT SIGNAL is available from the front panel BNC jack labeled OUTPUT and from the rear panel jack labeled FXD OUT. The source impedance is 50 ohms and the amplitude is nominally 1 volt rms with no load or 0.5 volts rms into a 50 ohm load.

For units equipped with Option 04, the amplitude of the OUTPUT SIGNAL with no load is nominally 10 volts peak-to-peak (3.6 volts rms) or 5 volts peak-to-peak into a 50 ohm load. It should be noted from the specification chart that the harmonic components for a unit equipped with Option 04 are greater than those for the standard unit.



1. POWER SWITCH
2. POWER INDICATOR
3. OUTPUT SIGNAL JACK



1. OUTPUT SIGNAL JACK
2. CRYSTAL ADJUST (OPTION -06)
3. LINE CORD
4. LINE SELECTOR SWITCH
5. FUSE HOLDER
6. PROGRAMMING JACK
7. EXT. REFERENCE INPUT
8. CRYSTAL ADJUST (OPTION -01)
9. REFERENCE OUTPUT

FIGURE 2.1 FRONT AND REAR PANELS

2.3 EXTERNAL REFERENCE

The standard unit is supplied with no internal crystal reference oscillator. Two optional 8 MHz oscillators are available as described in the specifications. Either of these oscillators may be phase-locked to an external 1 MHz reference signal. If neither of these oscillators is chosen, then an external 8 MHz reference signal must be provided. The rear panel BNC jack labeled REF IN accepts either the 1 MHz or 8 MHz external reference input signals.

2.3.1 EXTERNAL 8 MHz REFERENCE INPUT

An external 8 MHz reference signal is required for units without an internal crystal oscillator, but this signal may also be used to replace the signal from an internal oscillator when supplied.

The 8 MHz reference signal enters the rear panel BNC jack labeled REF IN.

NOTE

For external 8 MHz reference input operation, the INPUT REFERENCE SELECTOR JUMPER must be in the EXT position. This jumper is located inside the unit on the motherboard as shown in Figure 5.1.

The receiving circuit is a TTL Schmitt-trigger exhibiting a hysteresis characteristic with a positive-going threshold of 2 volts maximum and a negative-going threshold of 0.6 volts minimum. The waveform of the input signal must cross both thresholds for 50 nsec, minimum, once for each input cycle. The absolute maximum voltage limits are ±5.0 volts peak; loading is one standard TTL load.

2.3.2 PHASE-LOCKING TO AN EXTERNAL 1 MHz REFERENCE

If the unit is equipped with an internal crystal reference, then it may be phase-locked to an external 1 MHz reference input signal.

This signal enters via the rear panel BNC jack labeled REF IN and is conditioned by the same Schmitt trigger circuit described in section 2.3.1.

The pull-in range of the phase-locked loop is ± 2 Hz. As a check of proper phase-lock operation, follow section 3.7 of the Conformance Test Procedure. Failure to lock could be due to an excessive difference between the internal and external reference frequencies.

NOTE

For operation using the internal crystal reference oscillator, whether or not phase-locking is desired, the INPUT REFERENCE SELECTOR JUMPER must be in the INT position. This jumper is located inside the unit on the motherboard as shown in Figure 5.1.

When no external 1 MHz is connected to the REF IN jack, the internal crystal reference oscillator idles at its nominal frequency. This frequency may be adjusted as described in section 3.7 of the Conformance Test Procedure.

2.4 REFERENCE OUTPUT

The rear panel BNC jack labeled REF OUT provides a buffered TTL signal of either 8 MHz of 1 MHz, selectable by the OUTPUT REFERENCE SELECTOR JUMPER. This jumper is located inside the unit on the motherboard as shown in Figure 5.1. The buffer is capable of driving up to 30 standard TTL loads.

2.4.1 1 MHz REFERENCE OUTPUT

The OUTPUT REFERENCE SELECTOR JUMPER must be in the "1 MHz" position. The 1 MHz signal is a square wave derived either from the internal 8 MHz crystal reference oscillator or from the external 8 MHz reference input depending upon which is selected. See section 2.3.

2.4.2 8 MHz REFERENCE OUTPUT

The OUTPUT REFERENCE SELECTOR JUMPER must be in the "8 MHz" position, and the INPUT REFERENCE SELECTOR JUMPER must be in the INT position. The 8 MHz signal is a buffered version of the internal crystal reference oscillator and is a pulse waveform. When an external 8 MHz reference input is used, no 8 MHz reference output will be generated.

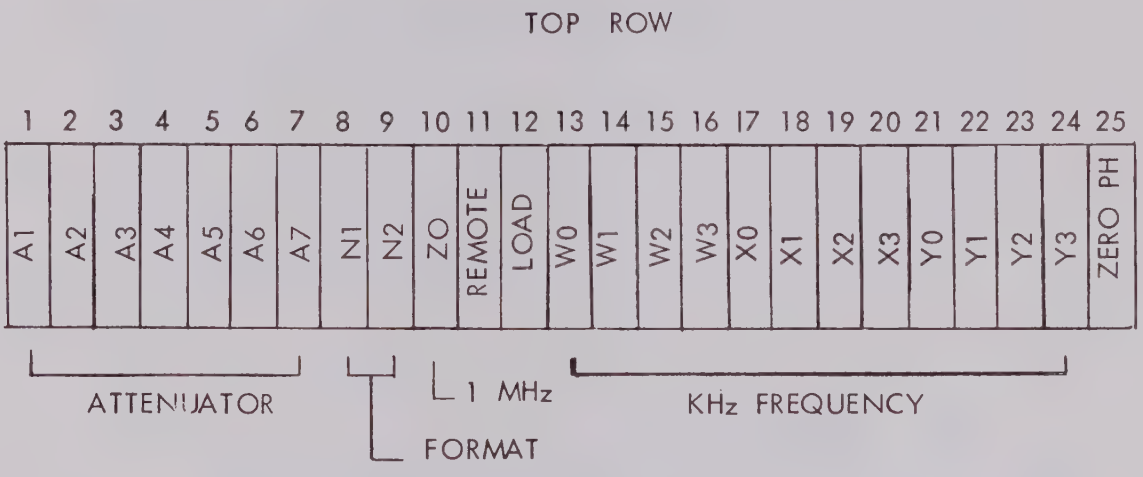
2.5 PHASE-LOCKING TWO MODEL 5110's

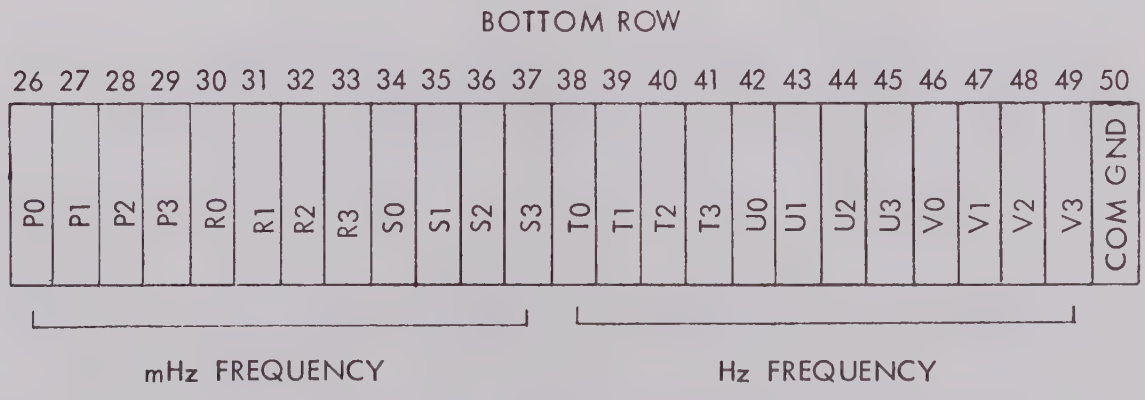
The recommended procedure for phase-locking two or more units is to use the 8 MHz reference output from one unit (chosen to be the master) as the 8 MHz reference input to the slave unit(s). The master unit may be phase-locked to an external 1 MHz signal if desired. See section 2.3.2.

2.6 PROGRAMMING CONNECTOR

All programming lines enter the rear panel 50-pin connector. The pin numbers shown on the connector and its mating plug (supplied) are identified in Figure 2.2.

FIGURE 2.2 REAR PANEL PROGRAMMING CONNECTOR - REAR VIEW


TOP ROW
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
A1 A2 A3 A4 A5 A6 A7 N1 N2 ZO REMOTE LOAD W0 W1 W2 W3 X0 X1 X2 X3 Y0 Y1 Y2 Y3 ZERO PH
ATTENUATOR
1 MHz
FORMAT
KHz FREQUENCY



Notes:

1. All signals are referenced to pin 50 COM GND.
2. All lines are internally pulled to +5V by 3.3 Kohm resistors and assume logical "1" level if unconnected.
3. See figure 2.5 for Programming Chart.

2.6.1 LOGIC LEVELS FOR PROGRAMMING LINES

All lines require standard TTL logic levels:

Low = Logical "0" = 0.0 V to 0.8 V

High = Logical "1" = 2.0 V to 5.5 V

These voltages are referenced to the COM GND line.

2.7 ZERO PHASE LINE

The ZERO PHASE LINE differs from the other program lines in that it is a bi-directional, input-output line conventionally referred to as a "wired-or" buss. Figure 2.3 shows the internal circuitry associated with this line.

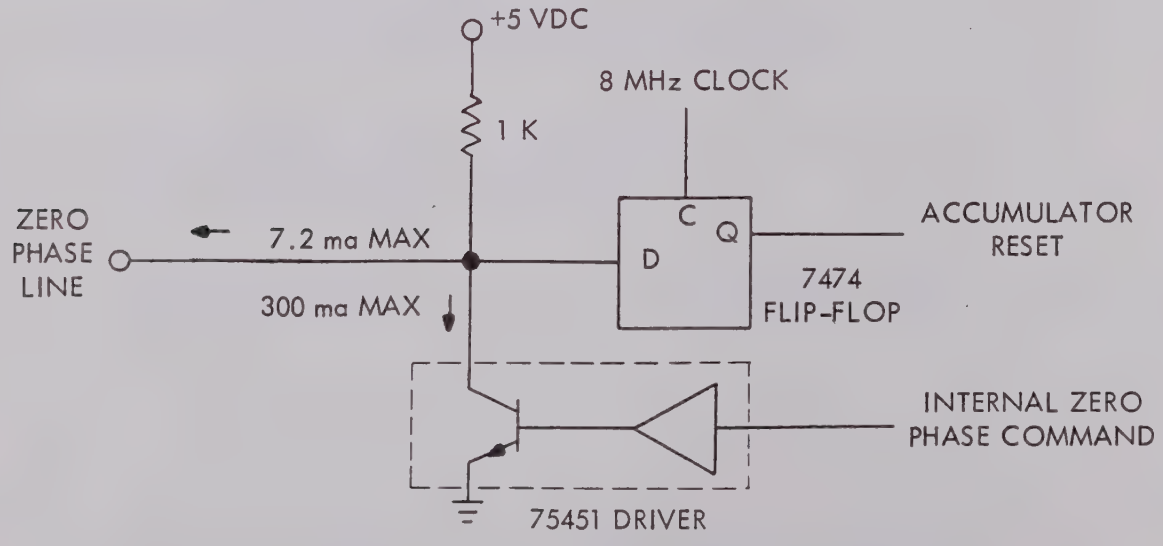


FIGURE 2.3 ZERO PHASE LINE CIRCUITRY

2.7.1 ELECTRICAL CHARACTERISTICS

The ZERO PHASE line is normally pulled to 5 V (logical "1") by the internal 1 K pull-up resistor. Either the internal NPN transistor or an external low impedance path to ground can pull this line to logical "0". This external driver should supply no current into the bus but only sink current to ground. If the external driver does supply current into the buss, this current must be limited to less than 300 ma and the driving circuit must be able to withstand a short to ground. Typical recommended drivers are: switch closure to ground, DTL logic, open-collector TTL logic, NPN transistor in common-emitter configuration, diode sink to ground, etc.

2.7.2 PHASE CONTROL

The ZERO PHASE line is sampled every 125 nsec by the D flip-flop shown in Figure 2.3. The output of this flip-flop controls the ACCUMULATOR RESET line. When this line is at logical "0" the phase value of the phase accumulator is set to zero degrees. When the line returns to logical "1", the phase accumulator begins advancing in value from the zero degree point.

There is a time uncertainty between the ZERO PHASE signal and the ACCUMULATOR RESET signal of up to 125 nsec. The duration of the ACCUMULATOR RESET signal will be an integral number of 125-nsec periods. Typically, there is a delay of 800 nsec between the ZERO PHASE line signal and the synthesizer output response.

2.7.3 LOAD ACKNOWLEDGE

As an output line, the ZERO PHASE line will acknowledge the loading of program data as described in sections 2.10.1 through 2.10.3. The internal NPN transistor will pull this line to logical "0" during the processing cycle causing a zero phase interval in the OUTPUT signal.

2.8 PROGRAMMING LINES

All programming lines except for the ZERO PHASE line have the input circuitry shown in Figure 2.4.

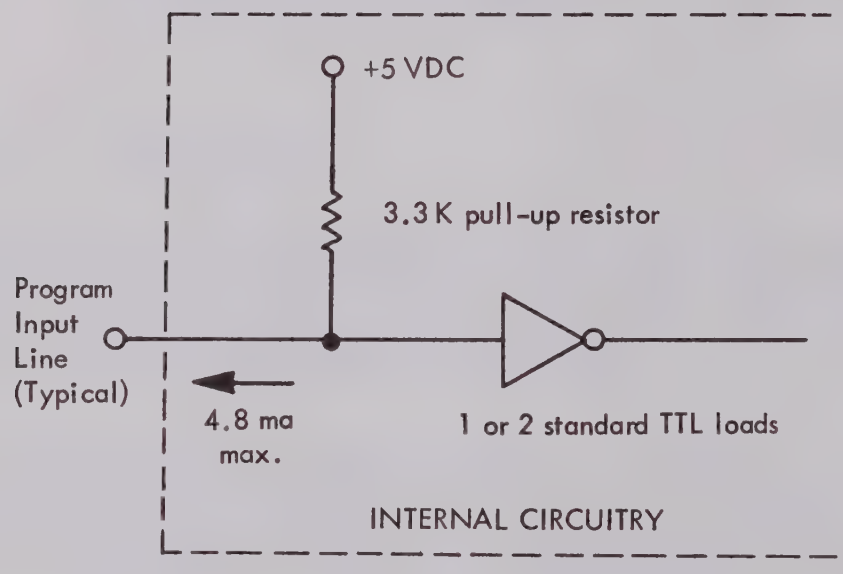


FIGURE 2.4 STANDARD PROGRAM LINE CIRCUITRY

Each programming line must sink a maximum of 4.8 ma when connected to ground potential. If a line is left unconnected, it will be internally pulled to +5 volts (logical "1") by the 3.3K pull-up resistor.

The programming lines can be divided into two categories: control lines and data lines. Control lines are used to set data format, initate loading, etc. The data lines set the value of the frequency or attenuation.

2.9 CONTROL LINES

The control lines are: ZERO PHASE, LOAD, REMOTE N1 and N2. The ZERO PHASE line is discussed in section 2.7 since it is a special line.

2.9.1 REMOTE LINE

The REMOTE line is used as a device select or a load enable line. When this line is at logical "1", all programming is defeated and the unit operates at its previously-loaded frequency. When this line is set to logical "0", loading is enabled as described below. If this line is not to be used, then it should be hardwired to logical "0" or COM GND.

NOTE

The ZERO PHASE line will operate regardless of the state of the REMOTE line.

2.9.2 LOAD LINE

The LOAD line initiates a load sequence, which transfers program data from the data lines into the internal data register. The line is normally at logical "1" and the falling edge of a negative-going pulse causes a load. The positive-going edge is ignored with the restriction that the pulse width is 50 nsec minimum.

2.9.3 N1 AND N2 LINES

There are four basic formats for loading data as shown in the following chart:

N1	N2	MODE
0	0	BINARY - WORD
1	0	BINARY - BYTE
0	1	BCD - WORD
1	1	BCD - BYTE

The WORD mode allows a single, parallel load of all data while the BYTE mode allows the user with a limited number of programming lines to load four 12-bit bytes sequentially. The weights of the programming lines may be either in BINARY or BCD format. Selection of these modes is accomplished by setting bits N1 and N2 to the proper level prior to entering a LOAD pulse. If only one mode is used, these bits may be permanently hardwired. Each of the four modes is described below and summarized in Figure 2.5.

2.10 DATA LINES

The frequency range of the unit is from DC to 2 MHz, with 1 MHz resolution throughout. Frequency data is divided into four ranges:

Range	Minimum	Maximum	Resolution
mHz	0 mHz	999 mHz	1 mHz
Hz	0 Hz	999 Hz	1 Hz
KHz	0 KHz	999 KHz	1 KHz
MHz	0 MHz	1 MHz	1 MHz

The programming chart in Figure 2.5 shows how data is formatted and weighed in each mode.

2.10.1 BINARY-WORD MODE

In this mode, N1 = N2 = logical "0", as shown in the MODE SELECT column in Figure 2.5. All lines are loaded with a single load pulse. The weight of each program line is shown beneath each line designation. Positive logic is used: a logical "1" on any of the lines will cause a contribution to the frequency equal to the weight of that line. Any binary number less than or equal to $999_{10} = 1111100111_2$ is valid for each of the three frequency ranges (KHz, Hz, and mHz). The lines Y_2, Y_3, V_2, V_3, S_2 and S_3 are unused in this mode and may be left unconnected. Any lines which are always to be logical "0" are simply hard-wired to GND.

The BINARY-WORD mode is the only programming mode which maintains phase and amplitude continuity between frequencies. Frequency sweeping is easily accomplished by causing repetitive loads of successively higher (or lower) frequencies. Although the frequency changes in discrete steps, each step can be as small as 0.001 Hz allowing a close approximation to a linear sweep in most applications.

The delay from the negative edge of the LOAD pulse to the change in frequency at the OUTPUT jack is approximately 1.5 usec. LOAD pulses may be accepted at a maximum rate of one per 0.625 usec. Data must be held valid until at least 0.625 usec after the negative edge of the LOAD pulse. The ZERO PHASE line is logical "1" during all BINARY-WORD loads. These conditions are indicated on the timing diagram in Figure 2.6.

2.10.2 BCD-WORD MODE

In this mode, N1 = logical "0" and N2 = logical "1". Programming lines are weighted in BCD code. The total of the weights in any of the three ranges (KHz, Hz, and mHz) cannot exceed 999; otherwise, any combination of weights is valid. For example, the frequency 150 Hz could be programmed with several different sets of data: (1) 100 Hz + 40 Hz + 10 Hz, (2) 100 Hz + 40 Hz + 8 Hz + 2 Hz, (3) 80 Hz + 40 Hz + 20 Hz + 10 Hz, etc. By properly choosing data lines, the number of active programming lines may be minimized in certain applications.

Data must remain valid for at least 4.5 usec after the negative-going edge of each LOAD pulse. The internal data processing circuitry requires a maximum of 18.0 usec to process the BCD data after a load. During the last 13.5 usec of this interval, the ZERO PHASE line will go to zero volts. The instrument is ready to receive a new load after this time, as shown in Figure 2.6.

2.10.3 BCD-BYTE AND BINARY-BYTE MODES

The byte loading mode is provided expressly for the user who has a limited number of data lines. Four 12-bit bytes are required, each byte being loaded in 12-bit parallel form. The first byte loads the MODE SELECT bits (N1 and N2), the ATTENUATOR bits (A1 through A7, Option 02 only) and the 1 MHz bit (Z_0) on the lines shown in Figure 2.5. A LOAD pulse causes loading of this data and initiates a wait cycle holding the ZERO PHASE line (and OUTPUT signal) at zero until the next three bytes have been loaded and processed. Data must be held valid for at least 4.5 usec after the first LOAD pulse.

The remaining three bytes program the mHz, Hz and KHz in that order, as shown in Figure 2.5. Each range (mHz, Hz, and KHz) is constrained exactly as in the word modes. The fourth LOAD pulse initiates processing of all loaded data after which the new signal appears at the output jacks. Data must be held valid for at least 375 nsec after each of the last three LOAD pulses.

Since the first byte and the remaining three bytes are loaded on two separate sets of lines, the user may tie these two sets in parallel, allowing a single set of 10 or 12 lines to serve for all byte inputs. These sets of lines are arranged adjacent to each other on the rear panel connector (see Figure 2.2) so that pins #1 through #10 may be easily connected to pins #26 through #35, respectively. Pins #36 and #37 are then included with the above ten lines to form a total of twelve for BCD bytes. Note that if binary format is used, these latter two lines may be omitted thus requiring a total of only ten lines for data input.

MODE	MODE SELECT N1	MODE SELECT N2	ATTENUATOR A7	A6	A5	A4	A3	A2	A1	FREQUENCY	LOAD
PIN NUMBER →	8	9	7	6	5	4	3	2	1	10 ... 16 ... 45 ... 39 ...	
BINARY WORD	0	0	40	20	10	8	4	2	1	1 * * 512 256 128 64 32 16 8 4 2 1	SINGLE
			DB							MHz KHz Hz mHz	
BCD WORD	0	1	40	20	10	8	4	2	1	1 800 400 200 100 80 40 20 10 8 4 2 1 800 400 200 100 80 40 20 10 8 4 2 1 800 400 200 100 80 40 20 10 8 4 2 1	SINGLE
			DB							MHz KHz Hz mHz	
BINARY BYTE	1	0	40	20	10	8	4	2	1	1	LOAD 1
			DB							MHz	
										* * 512 256 128 64 32 16 8 4 2 1	LOAD 2
										mHz	
										* * 512 256 128 64 32 16 8 4 2 1	LOAD 3
										Hz	
										* * 512 256 128 64 32 16 8 4 2 1	LOAD 4
										KHz	
BCD BYTE	1	1	40	20	10	8	4	2	1	1	LOAD 1
			DB							MHz	
										800 400 200 100 80 40 20 10 8 4 2 1	LOAD 2
										mHz	
										800 400 200 100 80 40 20 10 8 4 2 1	LOAD 3
										Hz	
										800 400 200 100 80 40 20 10 8 4 2 1	LOAD 4
										KHz	

* NOT USED

FIGURE 2.5 REMOTE PROGRAMMING CHART

WAVETEK

TOLERANCES (EXCEPT AS NOTED) DECIMAL ± FRACTIONAL ± ANGULAR ±

SCALE

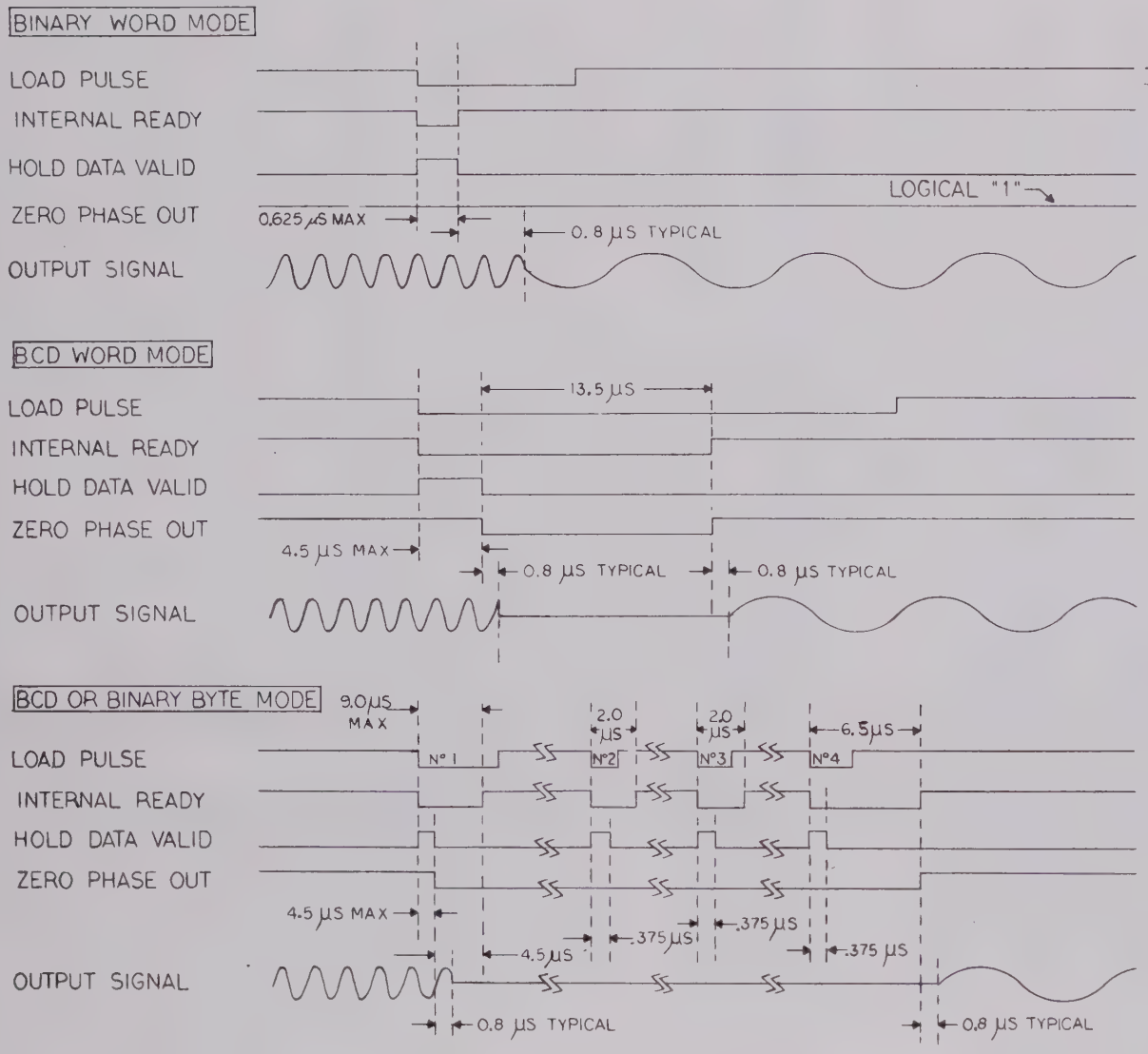
DRAWN BY JST APPROVED BY

TITLE REMOTE PROGRAMMING CHART

DATE 7-27-71 DRAWING NUMBER 510405 REV A

DATE	SYM	REVISION RECORD	AUTH	DR.	CK.
7/5/73	C	ECO 175			
7/18	D	ECO 223			
7/2	E	ECO 710			

OLD No 510406



NOTES:

1. ALL WAVEFORMS EXCEPT OUTPUT SIGNAL ARE SHOWN WITH STANDARD TTL LEVELS.
2. WHEN INTERNAL READY IS AT LOGICAL "1" A NEW LOAD PULSE WILL BE ACCEPTED.
3. DATA MUST BE HELD VALID DURING THE LOGICAL "1" PORTION OF HOLD DATA VALID.
4. POSITIVE-GOING EDGE OF LOAD PULSE IS IGNORED EXCEPT LOGICAL "0" INTERVAL IS 50 NSEC MIN.

FIGURE 2.6 TIMING DIAGRAM

TOLERANCES (EXCEPT AS NOTED)	WAVETEK		
DECIMAL XXX ±.010 XX ±.02		SCALE	DRAWN BY AST
			APPROVED BY
FRACTIONAL ± 1/64	TITLE TIMING DIAGRAM - LOADING		
ANGULAR ± 2°	DATE 6-15-73	DRAWING NUMBER 04-004-3100	REV E

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2.11 ATTENUATOR - OPTION 02

If Option 02 is elected, then the amplitude of the OUTPUT may be attenuated from its nominal maximum level of 1 volt rms (10 volts P-P for units also equipped with Option 04). Attenuation is selectable in 1 db increments from 0 db to 85 db. The attenuation level is programmed on lines A1 through A7 as shown in Figure 2.5. Internal registers store the data at the falling edge of the LOAD pulse and drive miniature relays to switch the appropriate resistor networks.

The settling time of the relay contacts is typically less than 5 msec. Protective circuitry insures that when switching between two levels of attenuation, the settling of the relays will never cause attenuation less than either of the two valid levels.

There is some degree of rolloff of attenuation at the higher frequencies. Figure 2.7 shows the actual attenuation as a function of frequency.

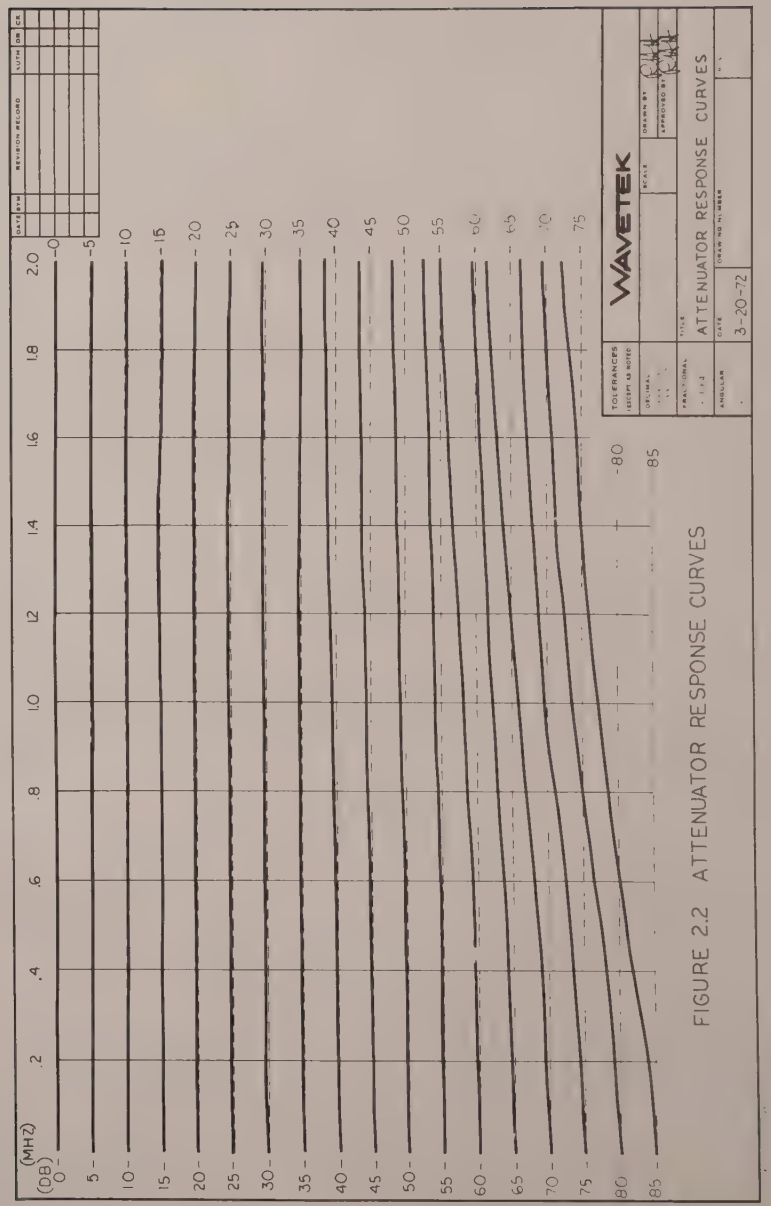


FIGURE 2.2 ATTENUATOR RESPONSE CURVES

SECTION 3 - CONFORMANCE TEST PROCEDURE

3.0 CONFORMANCE TEST PROCEDURE

This section describes procedures for verifying correct operation of the instrument and for making the necessary adjustments for optimum performance. If faulty operation is suspected, the steps in this section should be followed to determine the origin of the problem. Section 4 of this manual contains a trouble-shooting routine which is keyed to the steps in section 3. After each conformance test in section 3, there is a reference in parenthesis to a trouble-shooting (TS) chart in section 4.

Equipment required in the procedure is described below:

1. VARIAC (Variable autotransformer) - Voltage range = 0 to LINE, current = 1 amp.

2. OSCILLOSCOPE - Wideband (25 MHz), multi-channel (two channels minimum), vertical sensitivity =20 mV/cm, triggered sweep.

3. VOM - Capable of AC and DC voltage readings, 20,000 ohms/volt on DC.

4. RMS VOLTMETER - Calibrated in db, reads from +20 dbm to -80 dbm.

5. FREQUENCY COUNTER - Range 1 Hz to 2 MHz with 1 sec gating interval. Must accept 10 volt P-P sinewave.

6. PROGRAMMING DEVICE - Referred to as PGM. Capable of setting specified frequency and mode. Must generate a bounceless LOAD pulse. See section 2.

3.1 POWER SUPPLY

Equipment required for this test: VOM, Variac and oscilloscope. Refer to Figures 5.2, 5.8.1, and 5.8.2 for test points, component locations and schematic.

3.1.1 Initial Conditions VARIAC: Dial set at 0 volts.

3.1.2 Initial Conditions 5110: Line cord connected to VARIAC, power ON, PGM disconnected.

3.1.3 Connect negative probe of meter to ground bus at point A. Connect positive probe to point B and increase setting of VARIAC until a reading of +2.0 volts DC is reached. (TS 4.3)

3.1.4 Move positive probe to point C and verify +5 volts DC. (TS 4.3)

3.1.5 Move negative probe to point D, positive probe to point E and verify +5 volts DC. (TS 4.3)

3.1.6 Move negative probe to point A and positive probe to point B. Increase setting of VARIAC gradually, watching the meter climb to approximately +9 volts DC at full line voltage. (TS 4.3)

3.1.7 Initial Conditions Scope: Vertical sensitivity = 1 volt/cm, DC coupled, free-running sweep. Connect ground lead of scope probe to point A.

3.1.8 Connect tip of scope probe to points F, G, and H, reading 5.0 volts DC at each point. The trace must be "clean" with a maximum noise component of 200 mV P-P. (TS 4.4)

3.1.9 Set vertical sensitivity to 5 volts/cm on scope. Connect tip of probe to point J and verify +15 volts DC with 200 mV maximum noise. (TS 4.4)

3.1.10 Connect tip of probe to point K and measure -15 volts DC with 200 mV maximum noise. (TS 4.4)

3.2 CLOCK GENERATOR

Equipment required: Oscilloscope. Refer to Figure 5.2 for test point DC.

3.2.1 Initial Conditions 5110: Power ON, PGM disconnected, 8 MHz clock (internal or external) connected (see section 2.3).

3.4 DC OFFSET ADJUSTMENT

Equipment required: Oscilloscope, PGM. Refer to Figure 5.1 and 5.2 for location of parts and test points.

3.4.1 Initial Conditions 5110: PGM connected with ZERO PHASE line set to logical "0", power ON.

3.4.2 Initial Conditions Scope: Vertical sensitivity = 20 mV/cm, free-running sweep.

3.4.3 Connect a jumper between LPF IN and LPF GND.

3.4.4 Connect OUTPUT signal to scope and adjust R29 for zero volts DC.

3.4.5 Remove jumper between LPF IN and LPF GND.

3.4.6 Adjust R55 for zero volts DC. (TS 4.14)

3.5 BINARY-WORD MODE AND ACCUMULATOR

Equipment required: Frequency counter, PGM. Refer to Figure 5.2 for component locations.

3.5.1 Initial Conditions 5110: Power ON, PGM connected, ZERO PHASE line at logical "1", BINARY-WORD mode, REMOTE line at logical "0", set frequency bits as directed.

3.5.2 Connect frequency counter to OUTPUT signal, 1 second gate interval.

3.5.3 Set each of the Hz bits from 1 Hz to 512 Hz to logical "1" and load for each bit. Verify the correct frequency on the counter for each bit. (TS 4.6)

3.5.4 Repeat step 3.5.3 with KHz bits and the 1 MHz bit. (TS 4.6)

3.5.5 Return all frequency bits to logical "0".

3.5.6 Remove the Hz carry jumper shown in Figure 5.1. Connect the blue mHz carry jumper supplied in the plastic bag from point MT to point MC.

3.5.7 Repeat step 3.5.3 with the mHz bits, reading the frequency on the counter in Hz for a setting in mHz on the PGM. (TS 4.6)

3.5.8 Remove the blue mHz carry jumper and replace the small, black Hz carry jumper.

3.6 BYTE AND BCD-WORD MODES

Equipment required: Frequency counter, PGM.

3.6.1 Initial Conditions 5110: Power ON, PGM connected, ZERO PHASE line at logical "1", REMOTE line at logical "0", mode and frequency bits as directed.

3.6.2 Connect OUTPUT signal to frequency counter with 1 second gate interval.

3.6.3 Set PGM to BCD-WORD mode and set each of the Hz and KHz bits from 1 Hz through 800 KHz to logical "1" and enter LOAD pulse for each. Verify the correct frequency on the counter for each bit. (TS 4.10)

3.6.4 Remove the black Hz carry jumper and connect the blue mHz carry jumper supplied in the plastic bag from point MT to point MC as shown in Figure 5.1.

3.6.5 Set each of the mHz bits from 1 mHz to 800 mHz to logical "1" and enter LOAD pulse for each. Verify the correct frequency on the counter in Hz for a setting on the program lines in mHz. (TS 4.10)

3.6.6 Set PGM to BINARY-BYTE. Set PGM lines to logical "1" for 512, 128, 32, 8, and 2 mHz. Enter three (3) LOAD pulses. Set mHz lines previously loaded to logical "0" and set 256, 64, 16, 4, and 1 mHz lines to logical "1". Enter one LOAD pulse. Counter should read 341, 682 Hz. (TS 4.11)

3.6.7 Remove the blue mHz carry jumper and replace the small, black Hz carry jumper.

3.6.8 Set PGM to BCD-BYTE. Set PGM lines to logical "1" for 400, 100, 40, 10, 4, and 1 mHz, and also for 1 MHz. Enter three (3) LOAD pulses. Set the previously loaded lines to logical "0" and set 400, 200, 100, 80, 8, and 1 mHz lines to logical "1". Enter one LOAD pulse. Counter should read 1, 789, 555 Hz. (TS 4.11)

3.6.9 Set PGM to BINARY-WORD, set and LOAD a frequency of 1 KHz. Verify 1 KHz reading on counter.

3.6.10 Set REMOTE line to logical "1", set and LOAD a frequency of 2 KHz. Verify a 1 KHz reading maintained on counter.

3.7 INTERNAL OSCILLATOR ADJUSTMENT - OPTION 01 OR 06 ONLY

Equipment required: Oscilloscope, and an external 1 MHz frequency standard. The waveform of this signal is arbitrary but for each cycle it must enter the limits of logical "0" and logical "1" voltage levels. The absolute maximum limits are ±5 volts.

3.7.1 Initial Conditions 5110: Power ON, ZERO PHASE line at logical "0", INPUT REFERENCE SELECTOR JUMPER in the INT position, OUTPUT REFERENCE SELECTOR JUMPER in 1 MHz position. See Figure 5.1.

3.7.2 Initial Conditions Scope: Vertical sensitivity = 5 volts/cm, sweep = 100 nsec/cm, sync triggered on channel A.

3.7.3 Connect external 1 MHz standard to channel A of scope and adjust trigger to lock the waveform.

3.7.4 Connect the REF OUT signal from the 5110 rear panel to channel B. Verify a 1 MHz square-wave. (TS 4.12)

3.7.5 Locate the proper FREQ ADJ hole on the rear panel. With a small, non-metallic flat-bladed screwdriver, adjust the slug so that the waveform of channel B is stationary with respect to channel A. (TS 4.13)

3.7.6 Connect the 1 MHz standard to the REF IN jack on the rear panel of the 5110 and verify that the leading edges of the waveforms of channel A and channel B are phase-locked at 180°. (TS 4.13)

3.8 PROGRAMMABLE ATTENUATOR - OPTION 02 ONLY

Equipment required: PGM, RMS voltmeter.

3.8.1 Initial Conditions 5110: PGM connected, BINARY-WORD mode, power ON.

3.8.2 Set all PGM lines to logical "0" except ZERO PHASE and 1 KHz. Enter LOAD pulse.

3.8.3 Connect voltmeter to OUTPUT signal and take a reference for attenuation measurements. This reference should be approximately +3 dbm for standard units and +13 dbm for units equipped with Option 04.

3.8.4 Set attenuation bits to logical "1" for A1 through A7, one at a time and enter a LOAD pulse for each bit. Verify the correct attenuation level for each bit to within ±.5 db. (TS 4.15)

SECTION 4- TROUBLE-SHOOTING

4.0 TROUBLE-SHOOTING

In the event of a malfunction, a mechanical inspection is advised before proceeding with the trouble-shooting section.

4.1 INSTRUCTIONS FOR USE OF THE TROUBLE-SHOOTING CHART

4.1.1 If trouble develops, start with the CONFORMANCE TEST PROCEDURE (CTP) in section 3, following it until a discrepancy is found. Refer to the TS (Trouble-Shooting) section which appears in parenthesis after the non-conforming item and start trouble-shooting at this section in the TROUBLE-SHOOTING CHART.

4.1.2 Set up the TEST CONDITIONS, connect the appropriate instrument to the TEST POINT and verify results in each OBSERVATION row. If the OBSERVATION description is verified, continue downward to the next OBSERVATION, changing TEST CONDITIONS and TEST POINT as necessary.

4.1.3 If the OBSERVATION is not verified, refer to the REMEDY column in that row. Perform each part of the REMEDY instructions one at a time and recheck the results with the OBSERVATION column until OBSERVATION checks.

4.1.4 When the results are corrected, return to the CTP and recheck the test which failed previously. If the test still fails, return to the TROUBLE-SHOOTING CHART and resume testing with the LAST step performed above.

4.1.5 If the trouble is not found after exhausting the steps within one section, do not continue into the next section. Rather, return to the CTP and repeat all tests made to that point, hopefully uncovering some earlier discrepancy not noticed before.

4.1.6 a. Part designations may be found on the assembly drawings in section 5. The assemblies are numbered as follows:

A 1 - Main PC Board (Motherboard) Assembly

A 3 - Attenuator Board Assembly

A 4 - Front Panel Assembly

A 5 - Rear Panel Assembly

All part designations on Assembly A 1 will have no prefix, while parts on A 3, A 4, A 5 will have designations with these prefices.

4.1.6 b. Designations for pins on IC's are in the form of UXX-YY where XX is the IC number and YY is the pin number. Pin numbers for TOP views of the three sizes of IC package used are shown in Figure 4.1.

4.1.6 c. IC numbers on the motherboard are etched into bottom side of the PC board.

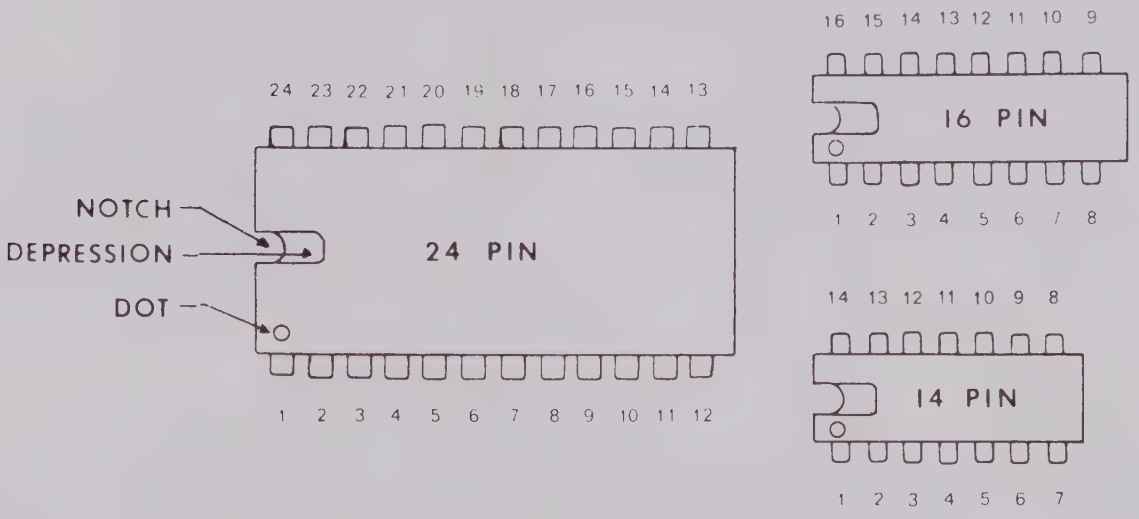


FIGURE 4.1 DIP PIN NUMBERING

4.2 FACTORY SERVICE

If the cause of the problem cannot be found, the factory should be consulted. A complete and accurate description of the problem should be made in order to help locate the cause. If the unit is to be returned to the factory, a written and pictorial report should be enclosed to aid in duplicating the operating conditions under which the unit failed.

4.3 LOW OR UNREGULATED DIGITAL SUPPLY VOLTAGE

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. Power OFF		Check fuse	Replace if necessary
1. Power ON 2. Apply 5VAC across line cord (10VAC for units that are switched to 230VAC line power by the power selection switch on the back panel)	A5T1 PRI #1 0-115	Measure 5VAC	Check continuity of line cord, fuse holder, and power switch S2B. Replace if defective.
	A5T1 PRI #2 0-115	Measure 5VAC	
	A5T1 SEC #1 0-8	Measure 0.4VAC	1. If voltages are all zero, replace XFORMER A5T1. 2. If one or more voltages are low, check for shorts or opens in wiring to bridge rectifiers. 3. Check bridge rectifiers A5CR1, CR2, CR3.
	A5CR1 - AC Input		
	A5T1 SEC #2 0-16.5	Measure 0.75VAC	
	CR2 AC Input		
	A5T1 SEC #3 0-16.5	Measure 0.75VAC	
	CR3 AC Input		
	Across C1	Measure 0.8VDC	1. Check for shorted C1, C2, C3, Q1, Q2, Q3 and replace.
	Across C6	Measure 0.8VDC	1. Check for shorted C6, Q4, and replace.
	Across C7	Measure 0.8VDC	1. Check for shorted C7, Q5, and replace.

4.4 LOW OR ZERO REGULATOR VOLTAGE

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. Power ON 2. Normal line voltage	F	As per CTP 3.1.8	Replace Q3
	G	As per CTP 3.1.8	Replace Q2
	H	As per CTP 3.1.8	Replace Q1
	J	As per CTP 3.1.9	Replace Q4
	K	As per CTP 3.1.10	Replace Q5

4.5 CLOCK GENERATOR MALFUNCTION

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. PGM disconnected. 2. Power ON 3. 8 MHz clock (internal or external) connected.	U96-1	8MHz pulse waveform Option 01 or 06.	Check power supply voltages. Replace XTAL oscillator Y1.
	U7-6	Negative pulse waveform. $\overline{CLK}$. Width=40nsec; Period=125nsec.	Check U95, U89, U70, U81, U96
	U6-8	Negative pulse waveform. $\overline{ACLK}$. Width=40nsec; Period=125nsec.	Check U6, U7, U8, U9, U22
	U18-8	Negative pulse waveform. $\overline{BCLK}$. Width=40nsec; Period=500nsec.	Check U5, U4, U18, U70.
	U18-6	Negative pulse waveform. $\overline{CCLK}$. Width=40nsec; Period=1.5usec.	Check U17, U18, U19, U7.
	U19-6	Negative pulse waveform. $\overline{DCLK}$. Width=40nsec; Period 4.5usec.	Check U29, U18, U19, U53.
	U19-8	Negative pulse waveform. $\overline{ECLK}$. Width=40nsec; Period=4.5usec.	Check U19, U10.

4.6 SAMPLE GENERATOR MALFUNCTION

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. PGM Connected.	U98-11	Negative pulse waveform Width=40nsec; Period=125nsec.	Check U95, U89, U96, go to 4.5.
2. ZERO PHASE at logical "1"	U25-10	Negative pulse waveform Width=40nsec; Period=125nsec.	Check U95.
3. 8 MHz Clock (internal or external) connected.	U98-9	Logical "1"	1. Verify A5J1-25 (ZERO PHASE) is logical "1". If not, correct it. 2. Check U79, U98, U50.
1. Set PGM to: a. BINARY-WORD b. 1 mHz 2. Enter LOAD pulse.	Pins #12 to 15 on U12, U23, U35, U46, U55 U63, U72, U80 Pins #13 to 15 on U1.	Logical "0"	Go to Section 4.9
	U1-12	Logical "1"	
	U36-13	Positive pulse waveform. Width=125nsec; Period=125usec See Figure 5.4.	Check U2, U13, U24, U15, U26, U25, U3, U14.
1. Set PGM to 1 Hz. 2. Enter LOAD pulse.	Pins #12 to 15 on U1, U12, U23, U46, U55 U63, U72, U80 Pins #13 to 15 on U35.	Logical "0"	Go to Section 4.9
	U35-12	Logical "1"	
	U64-13	Positive pulse waveform. Width=125nsec; Period=125usec See Figure 5.4.	Check U36, U47, U56, U38, U49, U25, U37, U48, U57.
1. Set PGM to 1 KHz. 2. Enter LOAD pulse.	Pins #12 to 15 on U1, U12, U23, U35, U46 U55, U72, U80 Pins #13 to 15 on U63.	Logical "0"	Go to Section 4.9
	U63-12	Logical "1"	

(continued over)

4.6 (continued)

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
(continued)	U58-5	Positive pulse waveform. Width=125nsec; Period=125usec. See Figure 5.4.	Check U64, U73, U82, U66 U65, U74, U58, U84.
	U83-9	1 KHz square wave.	Check U83, U95, U82.

4.7 DAC-1, 2, OR 3 INCORRECT

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
			Check U85, U78, U86, U87, U88, U95, U90, U91, U92, U77, U68, U59, U67, U76, U84

4.8 DAC-4 THROUGH DAC-11 INCORRECT

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
			Check U90, U92, U93, U100, U101, U102, U103, U94.

4.9 INCORRECT FREQUENCY REGISTER CONTENTS - BINARY-WORD MODE

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. PGM Disconnected. 2. Connect U34-6, U34-7, and U34-8 together. 3. Connect U19-4 to U31-4. 4. Connect U22-1 to U22-7.	U10-9	Logical "1"	Check U22, U10, go to 4.5.
	U10-5	Positive pulse waveform. Width = 125nsec; Period = 4.5usec.	Check U31, U20, U10.
	U70-6	Logical "0"	Check U70, U62, U53.
	U60-8 U51-12 U51-6 U51-8	Negative pulse waveform. Width = 40nsec; Period = 4.5usec.	Check U34, U7, U4, U41, U40, U61, U52, U60, U51.
REMOVE ALL JUMPERS			

4.10 INCORRECT FREQUENCY REGISTER CONTENTS - BCD-WORD MODE

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. PGM Disconnected. 2. Connect jumper between U52-12 and U52-7. 3. Sync on negative edge of $\overline{D4}$ or U53-12.	U60-8 U51-12 U51-6	Negative pulse waveform. Width = 40nsec; spacing = 125nsec. Pulses blanked to logical "0" Portion of U53-12. There are 108 pulses within a period of U53-12	Check U60, U51, U52, U61, U41, U40, U4.
	U70-6	Same as U53-12.	Check U70, U62.

(continued over)

4.1.0 (continued)

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. Sync on negative edge of U53-14 or $\overline{D2}$.	U1-12 or QH	Pattern of "000000000001" repeated three times during logical "0" portion of $\overline{D2}$. Bit spacing is 125nsec. 36 bits during $\overline{D2}$.	Check U1, U12, U23, U35, U46, U55, U63, U72, U80, U39.
1. Sync on negative edge of U53-13 or $\overline{D3}$.	U80-2 or K	Pattern of "100001101100" repeated three times during logical "0" portion of $\overline{D3}$. Bit spacing is 125nsec. 36 bits during $\overline{D3}$.	Check U32, U30, U43, U54, U44, U42, U33, U40, U39.
REMOVE ALL JUMPERS			
Follow procedure in section 3.6.3.			Check U7, U40, U62, U70, U52, U51, U60.

4.11 INCORRECT FREQUENCY REGISTER CONTENTS - BYTE MODES

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
Follow procedure in section 3.6.6 and 3.6.8.			Check U9, U8, U7, U60.

4.12 NO 1 MHz OUTPUT

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
			Check U81, U97.

4.13 CRYSTAL CANNOT BE ADJUSTED INTO PROPER RANGE

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
			Check U96, U98, U91, C13.
			Replace XTAL Y1.

4.14 OUTPUT AMPLIFIER DEFECTIVE

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
		Refer to the schematic in figure 5.7.1 for DC voltage test points, and verify these voltages.	Replace defective components.

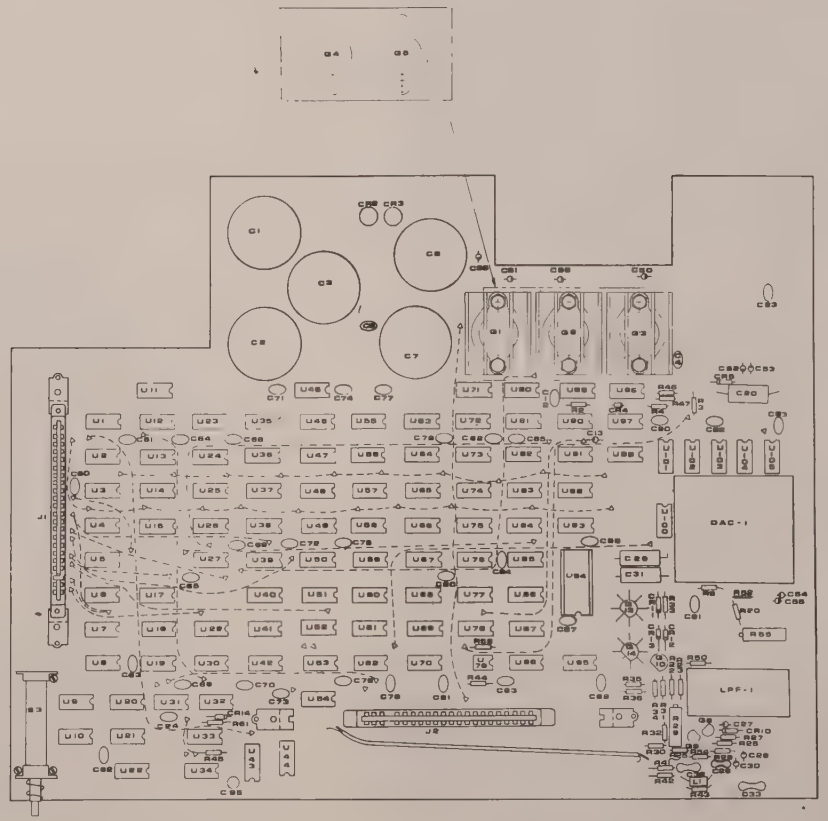
4.15 PROGRAMMABLE ATTENUATOR

TEST CONDITIONS	TEST POINT	CORRECT OBSERVATION	REMEDY
1. Power ON.	A3U8-14	+5 VDC	Replace A3Q1.
1. Disconnect Programmer. 2. Connect jumper from U31-4 or LD to U53-10 or DC. 3. Jumper from U22-1 to U22-7. 4. Jumper from U34-7 or W to U34-8.	A3U9-5	Negative pulse waveform. Width=125nsec; Period=4.5usec.	Check A2U9.
Follow procedure in section 3.8.		For errors in attenuation settings of: 1 db 2 db 4 db 8 db 10 db 20 db 40 db	Check following parts on assembly A3: A3-U2, -U1, -U9, -K1 A3-U2, -U3, -U10, -K2 A3-U3, -U4, -U10, -K3 A3-U4, -U5, -U11, -K4 A3-U6, -U5, -U11, -K5 A3-U6, -U7, -U12, -K6 A3-U8, -U7, -U12, -K7

SECTION 5 - SCHEMATIC AND ASSEMBLY DRAWINGS

Figure No.	Title
5.1	Motherboard Assembly A 1 - Component Side
5.2	Motherboard Test Points Assembly A 1 - Bottom Side
5.3	Basic Timing Signals
5.3.1	Timing Section Schematic
5.4	Accumulator Signals
5.4.1	Accumulator Section Schematic
5.5	ROM Address Signals
5.5.1	DAC Section Schematic
5.6	Motherboard Parts List
5.6.1	IC Manufacturer Cross Reference List
5.7	Output Amplifier Parts List
5.7.1	Output Amplifier Section Schematic
5.8	Power Supply Parts List
5.8.1	Power Supply Assembly A 5
5.8.2	Power Supply Section Schematic
5.9	Programmable Attenuator Parts List
5.9.1	Programmable Attenuator Assembly A 3
5.9.2	Programmable Attenuator Schematic

LTR	ECO NO.	CHANGED BY	APPV'D BY	DATE
A	RELEASE			
B	793 A			
C	906			



SHEET 2 IS "A" SIZE L/M

DRAWN BY	TH	DATE 6/6/86
CHECKED BY		
ENG APPVL		
MFG APPVL		

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AFTER FINISHING AND TOLERANCES ARE
XXX ± .005
XX ± .01
FRACTIONS ± 1/64
ANGLES ± 1°

WAVETEK

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TITLE: MAINBOARD ASSY. 5110 SERIES III

SIZE D | DRAWING NO 02 004-3110 | REV C

SCALE FULL | SHEET 1 OF 2

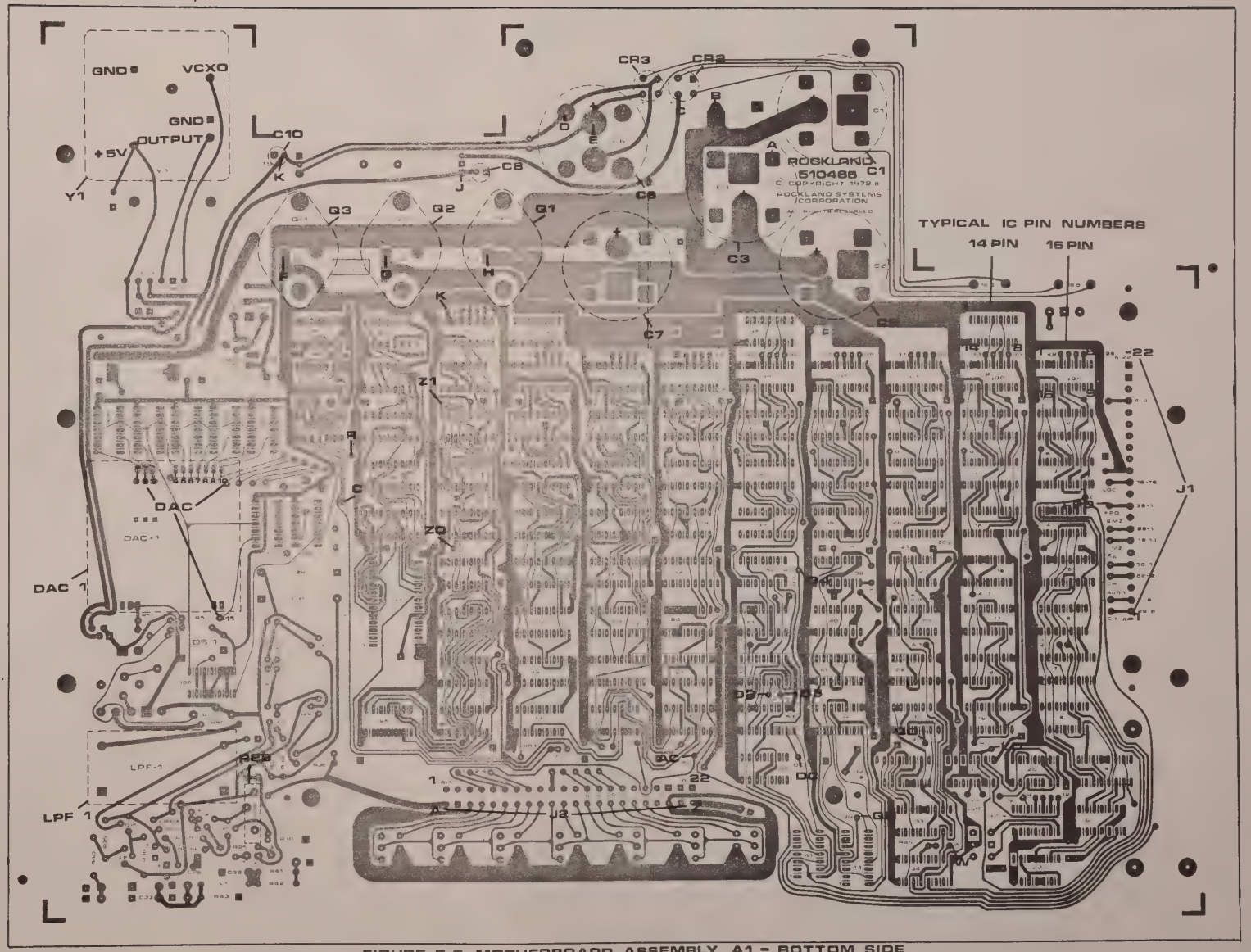
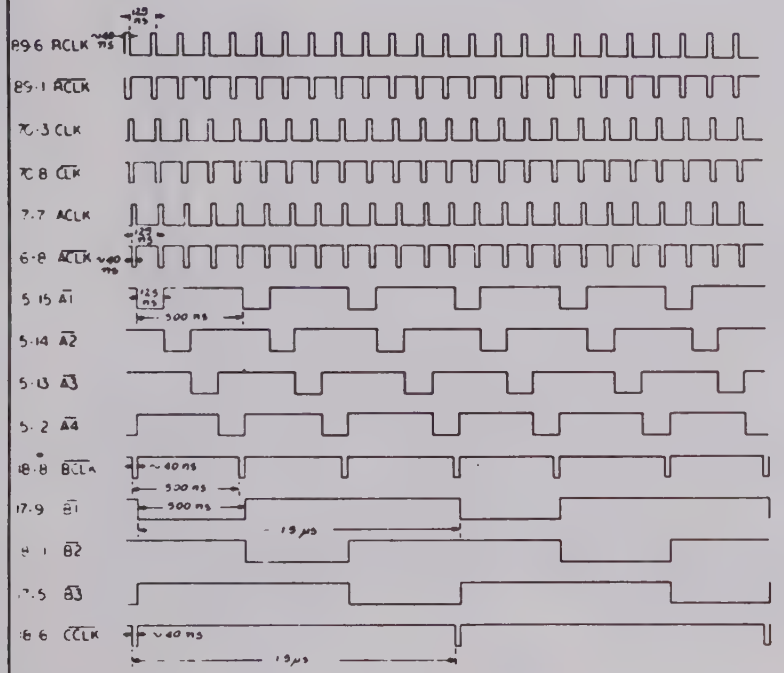
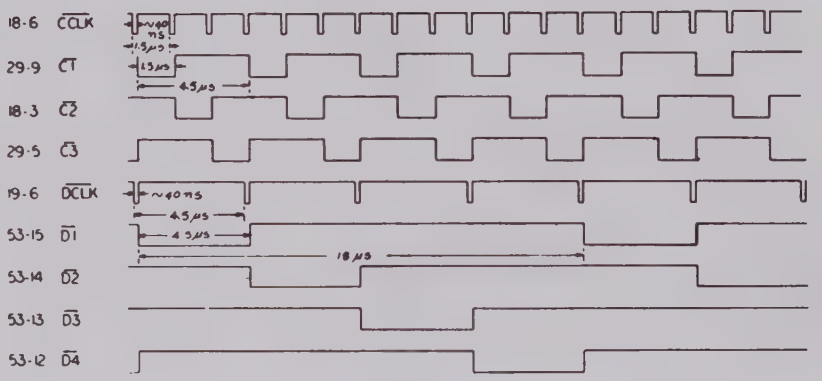


FIGURE 5.2 MOTHERBOARD ASSEMBLY A1 - BOTTOM SIDE





NOTES

D1 D2 D3 D4 ARE ACTIVE PULSE WAVEFORMS AS DRAWN ONLY DURING A CHANGE OF FREQUENCY. NORMALLY, D1 IS AT LOGICAL "0" AND D2 D3 D4 ARE AT LOGICAL "1"

TO CREATE A CONTINUOUS CHANGE OF FREQUENCY CONDITION TO OBSERVE ACTIVE D1 D2 D3 D4 REMOVE ASSEMBLY A2. ASSIGN A CLAMP FROM ITS CONNECTION

DESCRIPTION OF IC'S			
IC NO	PART NO	PINS TO VCC	PINS TO GND
4	122-7410	14	7
5	122-0106	16, 1	8
6	122-7404	14	7
7	22-9C15	16	8
8	122-7474	14	7
9	122-9C45	16	8
10	122-7474	14	7
16	122-74CX	14	7
17	122-7474	14	7
18	122-74CX	14	7
19	122-744C	14	7
20	122-7474	14	7
21	122-233C	14	
22	122-74CX	14	7
27	122-7474	14	7
28	122-74CC	14	7
29	122-7474	14	7
30	122-74CX	14	7
31	122-01CC	14	7

DESCRIPTION OF IC'S			
IC NO	PART NO	PINS TO VCC	PINS TO GND
32	122-9C15	16	1, 8, 15
33	122-9C15	16	1, 8, 15
34	122-0106	16	8, 9
39	122-7451	14	7
40	122-7400	14	7
41	122-7474	14	7
42	122-7474	14	7
43	122-8283	5	7, 8, 12
44	122-7474	14	7
50	122-74C4	14	7
51	122-7410	14	7
52	22-741C	14	7
53	122-0106	16	8
54	122-7474	14	7
60	122-7480	14	7
61	122-74CC	14	7
62	122-7410	14	7
70	122-7437	14	7

WAVETEK

FIGURE 5.3

		Issued	Drawn By J.T. Checked By PAR
	BASIC TIMING SIGNALS		
	Date 10-3-72		510431

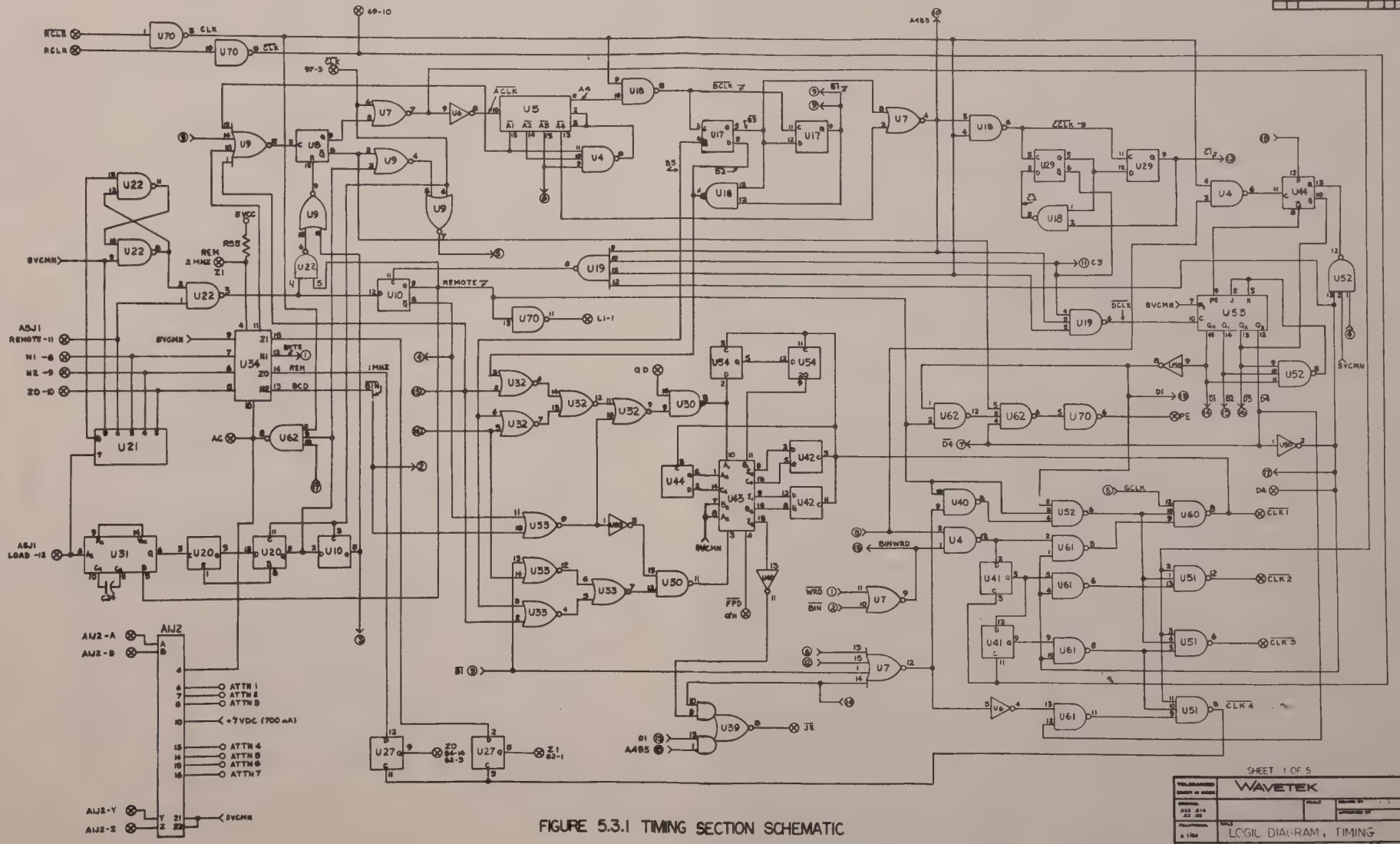
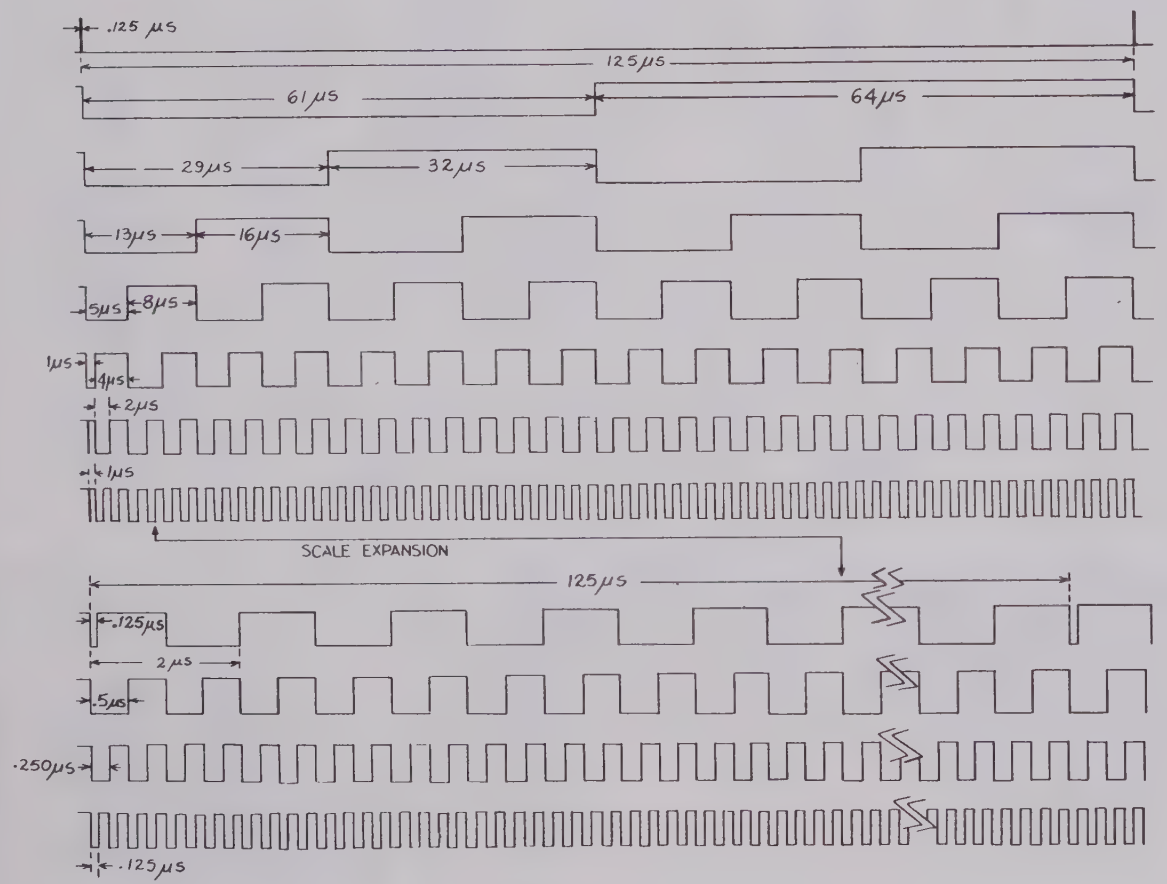


FIGURE 5.3.1 TIMING SECTION SCHEMATIC



SIGNAL LOCATION FOR GIVEN FRONT PANEL SETTING: 1 HZ	1 HZ	1KHZ
U36-13	U64-13	U58-5
U25-14	U57-13	U74-15
U25-13	U48-15	U74-14
U14-15	U48-14	U74-13
U14-14	U48-13	U74-12
U14-13	U48-12	U65-15
U14-12	U37-15	U65-14
U3-15	U37-14	U65-13
U3-15	U37-14	U65-13
U3-14	U37-13	U65-12
U3-13	U37-12	U57-15
U3-12	U25-15	U57-14

NOTES:

1. FOR EACH COLUMN, SET FREQUENCY SHOWN AND SYNC ON TOP WAVEFORM. VERIFY EACH SIGNAL FROM BOTTOM TO TOP.
2. IF TOP WAVEFORM IS MISSING OR INCORRECT, START WITH BOTTOM SIGNAL AND WORK UPWARDS UNTIL INCORRECT SIGNAL IS FOUND. START TROUBLE SHOOTING AT THIS POINT.

KEY:

— LOGICAL "1"
— LOGICAL "0"

FIGURE 5.4 ACCUMULATOR SIGNALS

WAVETEK

TOLERANCES (EXCEPT AS STATED): DECIMAL .XXX ±.010 .XX ±.02; FRACTIONAL ± 1/64; ANGULAR ±

SCALE 1:1 1/7

DRAWN BY QST

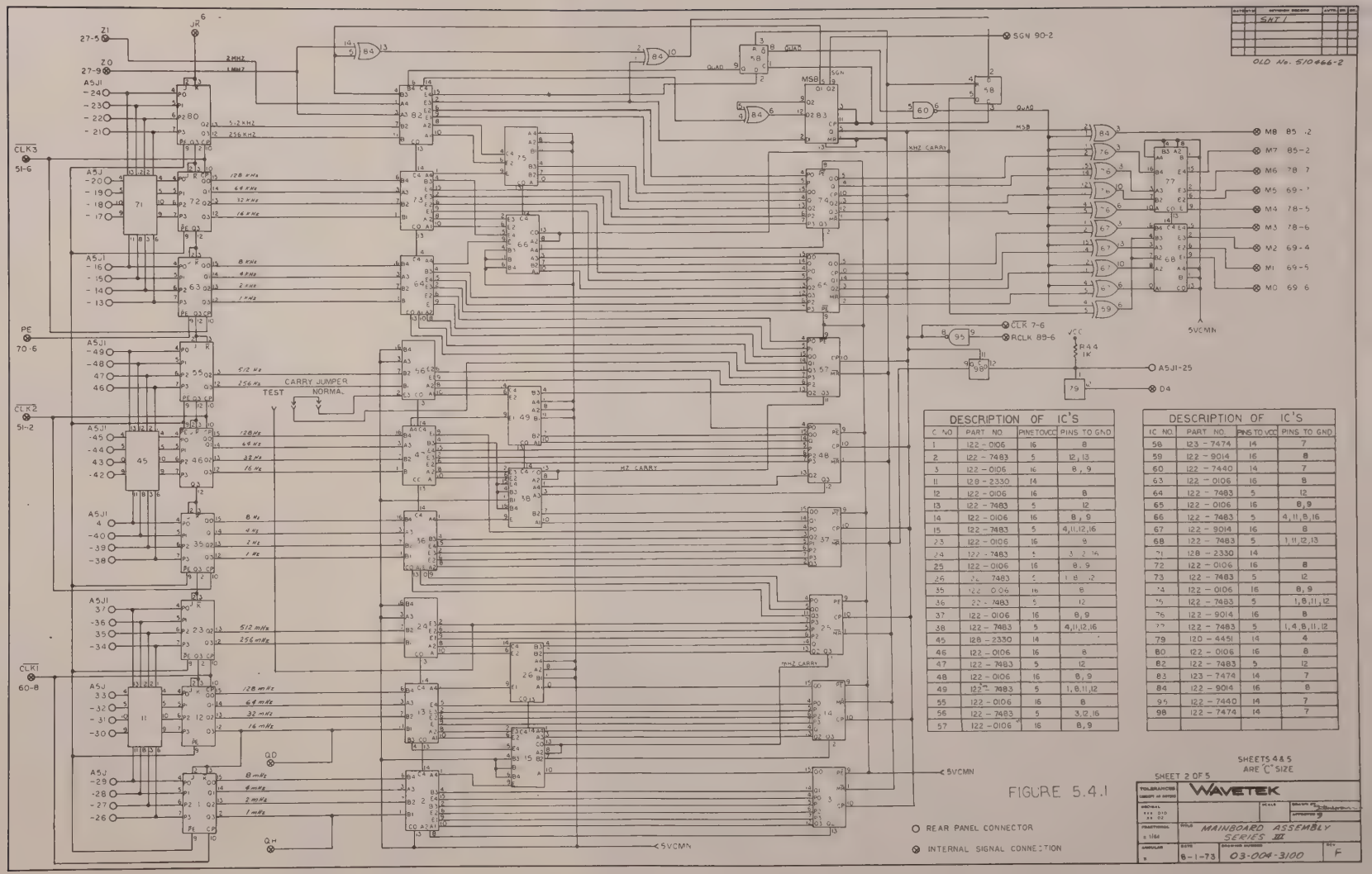
APPROVED BY

TITLE: ACCUMULATOR SIGNALS

DATE 10-9-72

DRAWING NUMBER 510441

REV



DESCRIPTION OF IC'S			
C NO	PART NO.	PINS TO VCC	PINS TO GND
1	122 - 0106	16	8
2	122 - 7483	5	12,13
3	122 - 0106	16	8, 9
11	128 - 2330	14	
12	122 - 0106	16	8
13	122 - 7483	5	12
14	122 - 0106	16	8, 9
15	122 - 7483	5	4,11,12,16
23	122 - 0106	16	8
24	122 - 7483	5	3,2,16
25	122 - 0106	16	8, 9
26	122 - 7483	5	1,8,12
35	122 - 0106	16	8
36	122 - 7483	5	12
37	122 - 0106	16	8, 9
38	122 - 7483	5	4,11,12,16
45	128 - 2330	14	
46	122 - 0106	16	8
47	122 - 7483	5	12
48	122 - 0106	16	8, 9
49	122 - 7483	5	1, 8, 11, 12
55	122 - 0106	16	8
56	122 - 7483	5	3,12,16
57	122 - 0106	16	8, 9

DESCRIPTION OF IC'S			
IC NO.	PART NO.	PINS TO VCC	PINS TO GND
58	123 - 7474	14	7
59	122 - 9014	16	8
60	122 - 7440	14	7
63	122 - 0106	16	8
64	122 - 7483	5	12
65	122 - 0106	16	8, 9
66	122 - 7483	5	4, 11, 8, 16
67	122 - 9014	16	8
68	122 - 7483	5	1, 11, 12, 13
71	128 - 2330	14	
72	122 - 0106	16	8
73	122 - 7483	5	12
74	122 - 0106	16	8, 9
75	122 - 7483	5	1, 8, 11, 12
76	122 - 9014	16	8
77	122 - 7483	5	1, 4, 8, 11, 12
79	120 - 4451	14	4
80	122 - 0106	16	8
82	122 - 7483	5	12
83	123 - 7474	14	7
84	122 - 9014	16	8
95	122 - 7440	14	7
98	122 - 7474	14	7

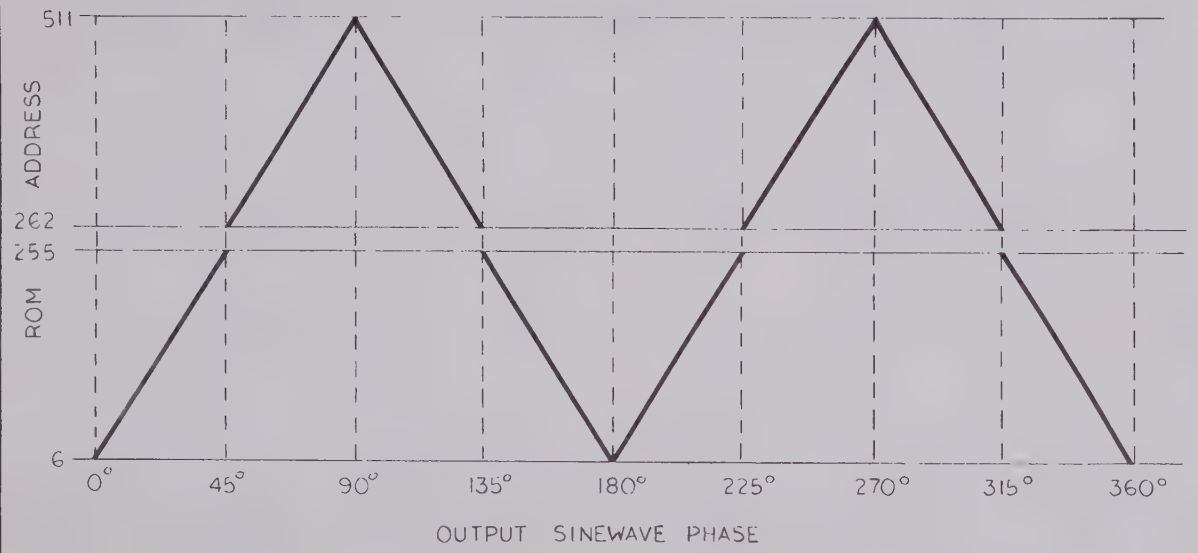
SHEETS 4 & 5 ARE "C" SIZE

SHEET 2 OF 5

FIGURE 5.4.1

TOLERANCES UNLESS OTHERWISE SPECIFIED	WAVETEK
DECIMAL .xx ±.010 .xxx ±.002	SCALE
FRACTIONAL ± 1/64	TITLE MAINBOARD ASSEMBLY SERIES III
ANGULAR ±	DATE 8-1-73
	DRAWING NUMBER 03-004-3100
	REV F

READ ONLY MEMORY (ROM) ADDRESS AS A FUNCTION OF SINEWAVE PHASE



DATE	BYM	REVISION RECORD	AUTH	DR.	CK

Address Bits	Location	Weight	Address Examples 38	144	265
ADR 0 (MSB)	U94-6	256	0	0	1
ADR 1	U94-5	128	0	1	0
ADR 2	U94-4	64	0	0	0
ADR 3	U94-3	32	1	0	0
ADR 4	U94-2	16	0	1	0
ADR 5	U94-1	8	0	0	1
ADR 6	U94-23	4	1	0	0
ADR 7	U94-22	2	1	0	0
ADR 8 (LSB)	U94-21	1	0	0	1

Logical "1" = 2.0 to 5.0 Volts

Logical "0" = 0.0 to 0.8 Volts

NOTES:
1. ROM IS ARRANGED IN 512 X 8 STRUCTURE. 500 WORDS ARE USED TO STORE RELATIVE MAGNITUDE OF SINE FUNCTION FROM 0° TO 90°. ADDRESSES 6 THROUGH 255 STORE 0° TO 45° AND ADDRESSES 262 THROUGH 511 STORE 45° THROUGH 90°.
2. ABOVE GRAPH SHOWS HOW ROM IS ADDRESSED TO PRODUCE 360° SINEWAVE. INVERSION AFTER ROM PROVIDES NEGATIVE OPERATION FOR 180° TO 360°.
3. WITH FRONT PANEL SETTING OF 4 KHZ ADDRESS IS INCREMENTED ONE STEP PER 125 NSEC = SAMPLING RATE. EACH ADDRESS STEP CORRESPONDS TO A PHASE STEP OF 0.18°. DURING ONE SINE CYCLE THERE ARE 2,000 SAMPLES. (2,000 X 0.18° = 360°)
4. EACH OF THE NINE ADDRESS BITS MAY BE MONITORED AND VERIFIED BY DISPLAYING DAC-1 ON SCOPE. SEE SECTION 3.3 AND FIGURE 3.3. DAC-1 HAS POSITIVE EDGE AT 0° PHASE OF THE OUTPUT SINEWAVE AND NEGATIVE EDGE AT 180°.
5. NON-CONFORMING ADDRESS BITS MAY BE DUE TO DEFECTIVE U69, U78, U85. OTHERWISE CHECK ACCUMULATOR MALFUNCTION.
6. SIGNALS DAC-4 THROUGH DAC-11 ARE GENERATED DIRECTLY FROM THE EIGHT OUTPUT BITS OF THE ROM. DAC-2 AND DAC-3 ARE SYNTHESIZED FROM DAC-4 AND ADR 8 THROUGH ADR 5. DAC-1 IS DERIVED DIRECTLY FROM THE ACCUMULATOR.

FIGURE 5.5

TOLERANCES (EXCEPT AS NOTED)			
DECIMAL XXX .010 XX .02		SCALE	DRAWN BY AST
			APPROVED BY
FRACTIONAL ± 1/64	TITLE ROM ADDRESS SIGNALS		
ANGULAR ±	DATE 11-17-72	DRAWING NUMBER 510408	REV

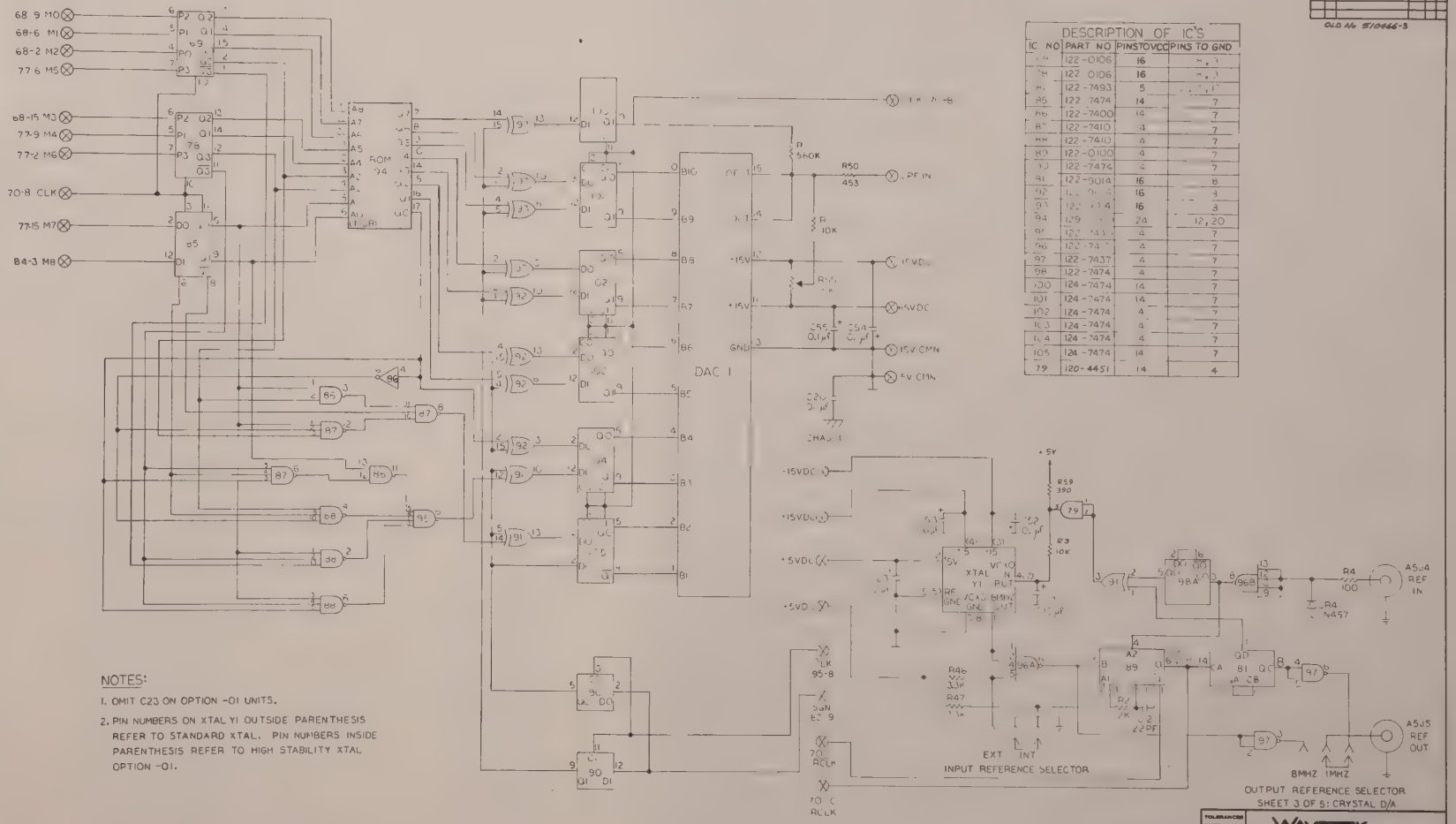

DESCRIPTION OF IC'S
IC NO | PART NO | PIN5TOVCC | PINS TO GND
122-0106 | 16
122 0106 | 16
122-7493 | 5
122 7474 | 14 | 7
122-7400 | 14 | 7
122-7410 | 4 | 7
122-7410 | 4 | 7
122-0100 | 4 | 7
122-7474 | 4 | 7
122-9014 | 16 | 8
16 | 3
16 | 3
129 | 24 | 12, 20
4 | 7
4 | 7
122-7437 | 4 | 7
122-7474 | 4 | 7
124-7474 | 14 | 7
124-7474 | 14 | 7
124-7474 | 4 | 7
124-7474 | 4 | 7
124-7474 | 14 | 7
120-4451 | 14 | 4
DAC 1
EXT INT
INPUT REFERENCE SELECTOR
OUTPUT REFERENCE SELECTOR
SHEET 3 OF 5: CRYSTAL D/A
SHEETS 4&5 ARE C SIZE
NOTES:
1. OMIT C23 ON OPTION -01 UNITS.
2. PIN NUMBERS ON XTAL Y1 OUTSIDE PARENTHESIS REFER TO STANDARD XTAL. PIN NUMBERS INSIDE PARENTHESIS REFER TO HIGH STABILITY XTAL OPTION -01.
WAVETEK
STANDARD
MAINBOARD ASSEMBLY SERIES III
6-13-73
03-004-3100
E

FIGURE 5.5.1

FIGURE 5.6 MOTHERBOARD INTEGRATED CIRCUITS PARTS LIST

Designation	Description	Rockland Part Number
U1	U: 4 bit shift register	122-0106
U2	U: 4 bit full adder	122-7483
U3	U: 4 bit shift register	122-0106
U4	U: triple 3 in NAND gate	122-7410
U5	U: 4 bit shift register	122-0106
U6	U: hex inverter	122-7404
U7	U: quad NOR gate	122-9015
U8	U: dual D type flip flop	122-7474
U9	U: quad NOR gate	122-9015
U10	U: dual D type flip flop	122-7474
U11	U: Pull up net 3.3K 2% x 13	128-2330
U12	U: 4 bit shift register	122-0106
U13	U: 4 bit full adder	122-7483
U14	U: 4 bit shift register	122-0106
U15	U: 4 bit full adder	122-7483
U17	U: dual D type flip flop	122-7474
U18	U: quad 2 in NAND gate	122-7400
U19	U: dual 4 in NAND buffer	122-7440
U20	U: dual D type flip flop	122-7474
U21	U: Pull up net 3.3K 2% x 13	128-2330
U22	U: quad 2 in NAND gate	122-7400
U23	U: 4 bit shift register	122-0106
U24	U: 4 bit full adder	122-7483
U25	U: 4 bit shift register	122-0106
U26	U: 4 bit full adder	122-7483
U27	U: dual D type flip flop	122-7474
U29	U: dual D type flip flop	122-7474
U30	U: quad 2 in NAND gate	122-7400
U31	U: monostable multivibrator	122-0100
U32	U: quad NOR gate	122-9015
U33	U: quad NOR gate	122-9015
U34	U: 4 bit shift register	122-0106
U35	U: 4 bit shift register	122-0106
U36	U: 4 bit full adder	122-7483
U37	U: 4 bit shift register	122-0106
U38	U: 4 bit full adder	122-7483
U39	U: dual 2 in 2 w AOI gate	122-7451
U40	U: quad 2 in NAND gate	122-7400
U41	U: dual D type flip flop	122-7474
U42	U: dual D type flip flop	122-7474
U43	U: 4 bit full adder	122-7483

FIGURE 5.6 MOTHERBOARD INTEGRATED CIRCUITS PARTS LIST

Designation	Description	Rockland Part Number
U44	U: dual D type flip flop	122-7474
U45	U: pull up net 3.3K 2% x 13	128-2330
U46	U: 4 bit shift register	122-0106
U47	U: 4 bit full adder	122-7483
U48	U: 4 bit shift register	122-0106
U49	U: 4 bit full adder	122-7483
U50	U: hex inverter	122-7404
U51	U: triple 3 in NAND gate	122-7410
U52	U: triple 3 in NAND gate	122-7410
U53	U: 4 bit shift register	122-0106
U54	U: dual D type flip flop	122-7474
U55	U: 4 bit shift register	122-0106
U56	U: 4 bit full adder	122-7483
U57	U: 4 bit shift register	122-0106
U58	U: dual D type flip flop	123-7474
U59	U: quad XOR gate inverted output	122-9014
U60	U: dual 4 in NAND buffer	122-7440
U61	U: quad 2 in NAND gate	122-7400
U62	U: triple 3 in NAND gate	122-7410
U63	U: 4 bit shift register	122-0106
U64	U: 4 bit full adder	122-7483
U65	U: 4 bit shift register	122-0106
U66	U: 4 bit full adder	122-7483
U67	U: quad XOR gate inverted output	122-9014
U68	U: 4 bit full adder	122-7483
U69	U: 4 bit shift register	122-0106
U70	U: quad 2 in NAND buffer	122-7437
U71	U: Pull up net 3.3K 2% x 13	128-2330
U72	U: 4 bit shift register	122-0106
U73	U: 4 bit full adder	122-7483
U74	U: 4 bit shift register	122-0106
U75	U: 4 bit full adder	122-7483
U76	U: quad XOR gate inverted output	122-9014
U77	U: 4 bit full adder	122-7483
U78	U: 4 bit shift register	122-0106
U79	U: dual peripheral driver	120-4451
U80	U: 4 bit shift register	122-0106
U81	U: 4 bit counter	122-7493
U82	U: 4 bit full adder	122-7483
U83	U: dual D type flip flop	123-7474
U84	U: quad XOR gate inverted output	122-9014
U85	U: dual D type flip flop	123-7474

Figure 5.6 Motherboard Integrated Circuits Parts List

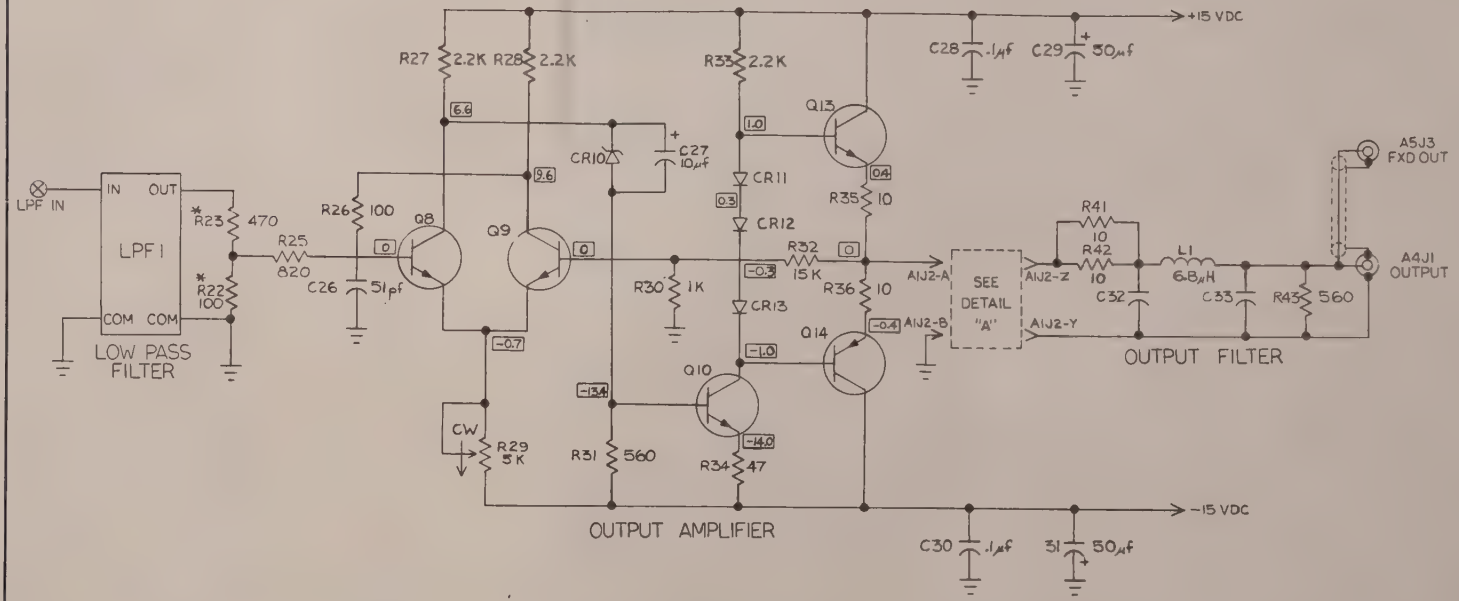
Designation	Description	Rockland Part Number
U86	U: quad 2 in NAND gate	122-7400
U87	U: triple 3 in NAND gate	122-7410
U88	U: triple 3 in NAND gate	122-7410
U89	U: monostable multivibrator	122-0100
U90	U: dual D type flip flop	122-7474
U91	U: quad XOR gate inverted output	122-9014
U92	U: quad XOR gate inverted output	122-9014
U93	U: quad XOR gate inverted output	122-9014
U94	U: ROM 512 x 8	129-3000
U95	U: dual 4 in NAND buffer	122-7440
U96	U: dual NAND Schmitt trigger	122-7413
U97	U: quad 2 in NAND buffer	122-7437
U98	U: dual D type flip flop	122-7474
U100	U: dual D type flip flop	124-7474
U101	U: dual D type flip flop	124-7474
U102	U: dual D type flip flop	124-7474
U103	U: dual D type flip flop	124-7474
U104	U: dual D type flip flop	124-7474
U105	U: dual D type flip flop	124-7474
R2	R: fxd metflm 2.0 K 1% 1/8 W	111-2000
R3	R: fxd comp 10 K 5% 1/4 W	116-3101
R4	R: fxd comp 100 ohm 5% 1/4 W	116-1101
R5	R: fxd comp 560 K 5% 1/4 W	116-4561
R20	R: fxd comp 10 K 5% 1/4 W	116-3101
R44	R: fxd comp 1 K 5% 1/4 W	116-2101
R45	R: fxd comp 3.3 K 5% 1/4 W	116-2331
R46	R: fxd comp 3.3 K 5% 1/4 W	116-2331
R47	R: fxd comp 3.3 K 5% 1/4 W	116-2331
R50	R: fxd metflm 453 ohm 1% 1/8 W	110-4530
R55	R: var cermet 5 K ±10% 3/4 W	118-2500
R59	R: fxd comp 390 ohm 5% 1/4 W	116-1391
C	C: fxd cer 0.1 uf + 80 - 20% 10 V	100-4100
C12	C: fxd mica dipped 22 pf 10% 500 V	101-0220
C13	C: fxd tant 10 uf 20% 25 V	109-6100
C20	C: fxd polyester 0.1 uf 10% 600 V	105-4100
C23	C: fxd cer 0.1 uf + 80 - 20% 10 V	100-4100
C24	C: fxd mica dipped 150 pf 10% 500 V	101-1150
C52	C: fxd tant 0.1 uf 20% 35 V	109-4100
C53	C: fxd tant 0.1 uf 20% 35 V	109-4100
C54	C: fxd tant 0.1 uf 20% 35 V	109-4100
C55	C: fxd tant 0.1 uf 20% 35 V	109-4100
CR4	CR: sil low leak 70 PIV	132-0457
DAC1	Converter: D/A 10 bit	004-3056
Y1	Oscillator: VCXO 8 MHz (Option -06)	173-6000
Y1	Oscillator: VCXO 8 MHz (Option -01)	173-6001

FIGURE 5.6.1 IC MANUFACTURER'S CROSS REFERENCE LIST

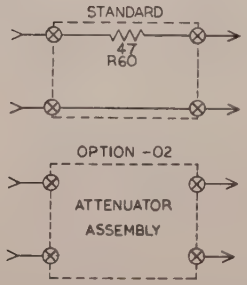
Rockland Part No.	Texas Inst.	Fairchild	National	Signetics
122-0100	SN74121N	74121 DC	DM74121N	N74121A
122-0102	SN74166N			N74166B
122-0106	SN74195N			
122-4451	SN75451P		LM75451A	
122-7400	SN7400N	7400 DC	DM7400N	N7400A
122-7404	SN7404N	7404 DC	DM7404N	N7404A
122-7410	SN7410N	7410 DC	DM7410N	N7410A
122-7413	SN7413N	7413 DC	DM7413N	N7413A
122-7437	SN7437N	7437 DC	DM7437N	N7437A
122-7440	SN7440N	7440 DC	DM7440N	N7440A
122-7451	SN7451N	7451 DC	DM7451N	N7451A
122-7474	SN7474N	7474 DC	DM7474N	N7474A
122-7493	SN7493N	7493 DC	DM7493N	N7493A
122-8283			DM8283N	N7483B
122-9014		9014 DC		
122-9015		9015 DC		
122-9328		9328 DC		N8277B
123-7474	SN74H74N	74H74 DC	DM74H74N	N74H74A
124-7440	SN74S40N	74S40 DC	DM74S40N	N74S40
124-7474	SN74S74N	74S74 DC	DM74S74N	N74S74
128-2330	Beckman No. 899-1-R3.3K			
129-3000	Custom Programmed ROM - Available only from			

FIGURE 5.7 OUTPUT AMPLIFIER PARTS LIST

	Designation	Description	Rockland Part Number
	C26	C: fxd mica 51 pf ±10% 500 WVDC	101-0510
	C27	C: fxd tant elect 10.0 MFD ±20% 25 WVDC	109-6100
	C28	C: fxd tant elect 0.1 MFD ±20% 35 WVDC	109-4100
	C29	C: fxd elect 50 MFD 25 WVDC	109-6500
	C30	C: fxd tant elect 0.1 MFD ±20% 35 WVDC	109-4100
	C31	C: fxd elect 50 MFD 25 WVDC	109-6500
	C32	C: fxd mica 1000 pf ±1% 500 WVDC	101-2101
	C33	C: fxd mica 1300 pf ±1% 500 WVDC	101-2131
	CR10	Diode: sil zener 20 V ±5% 400 MW	131-0200
	CR11	Diode: sil gen purp 70 PIV	132-0457
	CR12	Diode: sil gen purp 70 PIV	132-0457
	CR13	Diode: sil gen purp 70 PIV	132-0457
	L1	Inductor: fxd 6.8 UHY ±10%	168-5000
	LPF-1	Filter: low pass DC-2 MHz ±.25 db	165-3000
	Q8 & Q9	Transistor: silicon NPN matched pair	134-0065
	Q10	Transistor: silicon NPN	134-3568
	Q13	Transistor: silicon NPN	134-3568
	Q14	Transistor: silicon PNP	136-4354
*	R22	R: fxd comp 100 ohm ±5% 1/4 W	116-1101
*	R23	R: fxd comp 470 ohm ±5% 1/4 W	116-1471
	R25	R: fxd comp 820 ohm ±5% 1/4 W	116-1821
	R26	R: fxd comp 100 ohm ±5% 1/4 W	116-1101
	R27	R: fxd comp 2.2K ±5% 1/4 W	116-2221
	R28	R: fxd comp 2.2K ±5% 1/4 W	116-2221
	R29	R: var cermet 5K ±10% 3/4 W	118-2500
	R30	R: fxd met film 1K ±1% 1/8 W	111-1000
	R31	R: fxd comp 560 ohm ±5% 1/4 W	116-1561
	R32	R: fxd met film 15K ±1% 1/8 W	112-1500
	R33	R: fxd comp 2.2K ±5% 1/4 W	116-2221
	R34	R: fxd comp 47 ohm ±5% 1/4 W	116-0471
	R35	R: fxd comp 10 ohm ±5% 1/4 W	116-0101
	R36	R: fxd comp 10 ohm ±5% 1/4 W	116-0101
	R41	R: fxd comp 10 ohm ±5% 1/4 W	116-0101
	R42	R: fxd comp 10 ohm ±5% 1/4 W	116-0101
	R43	R: fxd comp 560 ohm ±5% 1/4 W	116-1561
	R60	R: fxd comp 47 ohm ±5% 1/4 W	116-0471
	* The following values pertain only to Option -04		
	R22	R: fxd met film 340 ohm ±1% 1/8 W	110-3400
	R23	R: fxd met film 221 ohm ±1% 1/8 W	110-2210



DETAIL "A"



NOTES

1 DC VOLTAGES ARE TYPICAL. ±10% VARIATIONS ARE NORMAL.
2 MEASUREMENTS MADE WITH A 20,000 Ω/V METER.
3 FREQUENCY SETTING: 0 HZ.
4 DC OFFSET ADJUSTED PER SECTION 3.4
5 RESISTORS IN OHMS
*6 FOR OPTION -04, R 23 IS 221 Ω, R 22 IS 340 Ω,

FIGURE 5.7.1 OUTPUT AMPLIFIER SECTION SCHEMATIC

SHEET 4 OF 5: ANALOG

TOLERANCES (UNLESS AS NOTED)	WAVETEK		
DECIMAL XXX .010 XX .02		SCALE	DRAWN BY / APPROVED BY
FRACTIONAL ± 1/64	TITLE MOTHERBOARD SCHEMATIC		
ANGULAR ±	DATE 11-13-73	DRAWING NUMBER 07-004-3110	REV A

FIGURE 5.8 POWER SUPPLY PARTS LIST

Designation	Description	Part Number
C1	C: Fxd, Elect, 10,000 MFD, 15WVDC	109-9100
C2	C: Fxd, Elect, 10,000 MFD, 15WVDC	109-9100
C3	C: Fxd, Elect, 10,000 MFD, 15WVDC	109-9100
C4	C: Fxd, Cer, 0.1 MFD, +80 - 20%, 10 V	100-4100
C5	C: Fxd, Cer, 0.1 MFD, +80 - 20%, 10 V	100-4100
C6	C: Fxd, Elect, 3,000 MFD, 50WVDC	109-8300
C7	C: Fxd, Elect, 3,000 MFD, 50WVDC	109-8300
C50	C: Fxd, Tant. Elect, 0.1 MFD ±20%, 35WVDC	109-4100
C51	C: Fxd, Tant. Elect, 0.1 MFD ±20%, 35WVDC	109-4100
C56	C: Fxd, Tant. Elect, 0.1 MFD ±20%, 35WVDC	109-4100
CR2	Rectifier: Silicon, FWB, 200 PIV, 1A	130-0140
CR3	Rectifier: Silicon, FWB, 200 PIV, 1A	130-0140
CR5	Rectifier: Silicon, 200 PIV, 1A	130-2110
CR6*	Rectifier: Silicon Zener 15V, 5%, 1W	131-0150
Q1	Regulator: Voltage, 5V ±10%	120-0051
Q2	Regulator: Voltage, 5V ±10%	120-0051
Q3	Regulator: Voltage, 5V ±10%	120-0051
Q4	Regulator: Voltage, 15V ±10%	120-0150
Q5	Regulator: Voltage, 15V ±10%	120-0150
A4S3	Switch: Push Button, Line	341-3100
A5B1	Fan: 115V, 15W	165-0701
A5C1	C: Fxd Ceramic .01 MFD, 1,000V	100-3100
A5C2	C: Fxd Ceramic .01 MFD, 1,000V	100-3100
A5CR1	Diode: Silicon, FWB, 50PIV, 12A	130-0541
A5F1	Fuse: 3AG 1A SB	165-4002
A5S1	Switch: Slide DPDT	342-2201
A5T1	Transformer: Power	177-3005

* Option -01 units only

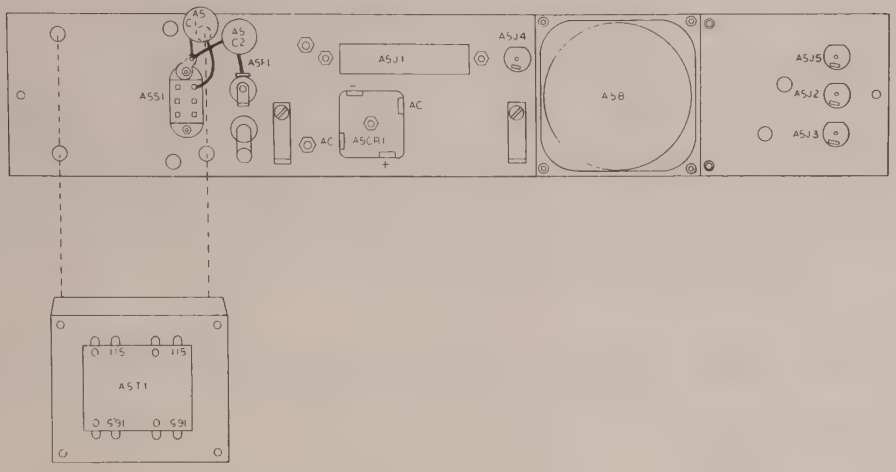
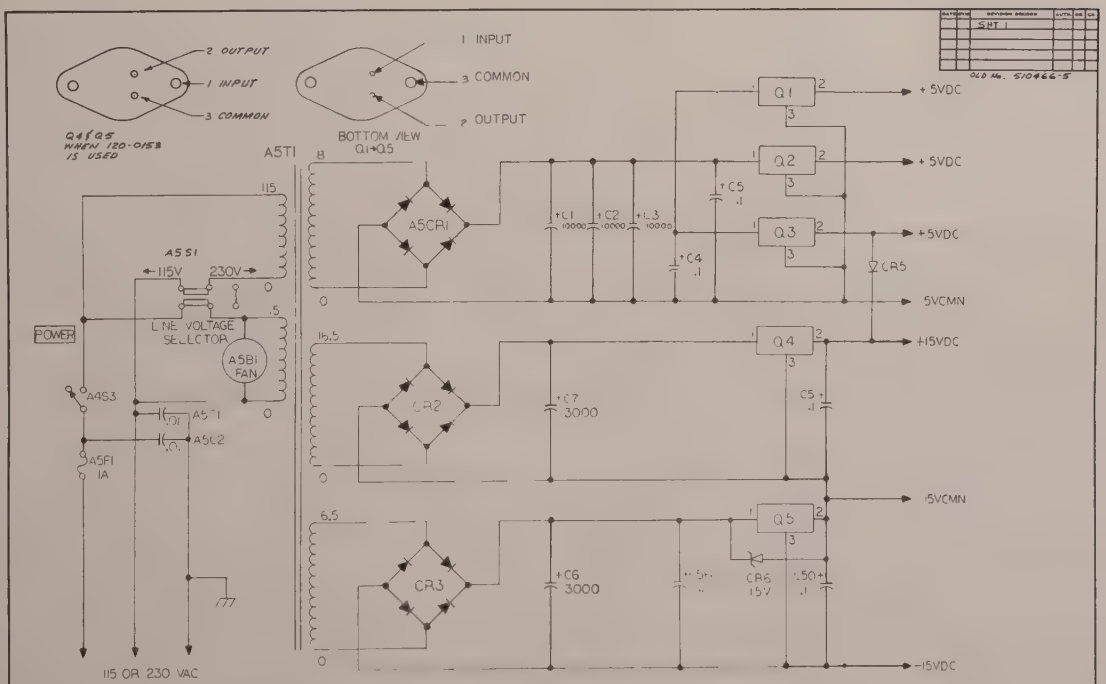


FIGURE 5.8.1 REAR PANEL ASSEMBLY

TOLERANCES	WAVETEK
DRAWN BY	AST
SCALE	1 / 1
TITLE	REAR PANEL ASSEMBLY A5
DATE	10 25 72
DRAWING NUMBER	510-4004
REV	B



NOTES:

1. REFERENCE DESIGNATION ARE ABREVIATED FOR ASSY A1
2. ALL CAPACITATOR VALUES ARE IN MICROFARADS
3. CR6 PRESENT ON OPTION -01 UNITS ONLY

SHEETS 1,2,3 ARE 'D' SIZE

SHEET 5 OF 5: POWER

FIGURE 5.8.2

TOLERANCES	WAVETEK
SCALE	
TITLE	MAINBOARD ASSEMBLY SERIES 200
DRAWING NUMBER	03 004-3100
REV	F

FIGURE 5.9 PROGRAMMABLE ATTENUATOR PARTS LIST

Designation	Description	Rockland Part Number
C1	C: Fxd, Tant. Elect., 0.1 MFD ±20%, 35WVDC	109-4100
C2	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C3	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C4	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C5	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C6	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
C7	C: Fxd, Tant. Elect., 10.0MFD ±20%, 25WVDC	109-6100
K1	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K2	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K3	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K4	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K5	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K6	Relay: Crystal, DPDT, 5V, 160MW	175-1502
K7	Relay: Crystal, DPDT, 5V, 160MW	175-1502
Q1	Regulator: Voltage, 5V ±10%	120-0050
R1	R: Fxd, Met.Flm, 49.9OHM ±1%, 1/8W	119-4990
R2	R: Fxd, Met.Flm, 887OHM ±1%, 1/8W	110-8870
R3	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R4	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R5	R: Fxd, Met. Flm, 887 OHM, ±1%, 1/8W	110-8870
R6	R: Fxd, Met. Flm, 432 OHM, ±1%, 1/8W	110-4320
R7	R: Fxd, Met. Flm, 11.3 OHM, ±1%, 1/8W	119-1130
R8	R: Fxd, Met. Flm, 432 OHM, ±1%, 1/8W	110-4320
R9	R: Fxd, Met. Flm, 221 OHM, ±1%, 1/8W	110-2210
R10	R: Fxd, Met. Flm, 23.7 OHM, ±1%, 1/8W	119-2370
R11	R: Fxd, Met. Flm, 221 OHM, ±1%, 1/8W	110-2210
R12	R: Fxd, Met. Flm, 115OHM, ±1%, 1/8W	110-1150
R13	R: Fxd, Met. Flm, 51.1 OHM, ±1%, 1/8W	119-5110
R14	R: Fxd, Met. Flm, 115OHM, ±1%, 1/8W	110-1150
R15	R: Fxd, Met. Flm, 97.6 OHM,±1%, 1/8W	119-9760
R16	R: Fxd, Met. Flm, 71.5 OHM,±1%, 1/8W	119-7150
R17	R: Fxd, Met. Flm, 97.6 OHM,±1%, 1/8W	119-9760
R18	R: Fxd, Met. Flm, 61.9 OHM,±1%, 1/8W	119-6190
R19	R: Fxd, Met. Flm, 249 OHM,±1%, 1/8W	110-2490
R20	R: Fxd, Met. Flm, 61.9 OHM,±1%, 1/8W	119-6190
R21	R: Fxd, Met. Flm, 51.1 OHM,±1%, 1/8W	119-5110
R22	R: Fxd, Met. Flm, 2.61K OHM,±1%, 1/8W	111-2610
R23	R: Fxd, Met. Flm, 51.1 K OHM, ±1%, 1/8W	119-5110
R24	R: Fxd, Comp., 1.0K OHM,±5%, 1/4W	116-2101
R25	R: Fxd, Comp., 2.2 K OHM, ±5%, 1/8W	116-2220
R26	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R27	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R28	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R29	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R30	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
R31	R: Fxd, Comp., 2.2K OHM, ±5%, 1/8W	116-2220
U1	I.C.: Dual D-Type Flip-Flop	122-7474
U2	I.C.: Quad 2-In Nand Gate	122-7400
U3	I.C.: Dual D-Type Flip-Flop	122-7474
U4	I.C.: Quad 2-In Nand Gate	122-7400
U5	I.C.: Dual D-Type Flip-Flop	122-7474
U6	I.C.: Quad 2-In Nand Gate	122-7400
U7	I.C.: Dual D-Type Flip-Flop	122-7474
U8	I.C.: Quad 2-In Nand Gate	122-7400
U9	I.C.: Dual Peripheral Driver	120-4451
U10	I.C.: Dual Peripheral Driver	120-4451
U11	I.C.: Dual Peripheral Driver	120-4451
U12	I.C.: Dual Peripheral Driver	120-4451

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK
20/3	A	ECO № 52			
JAN 8 '75	B	ECO 178			
JAN 8 '75	C	ECO 226			

OLD No 510345

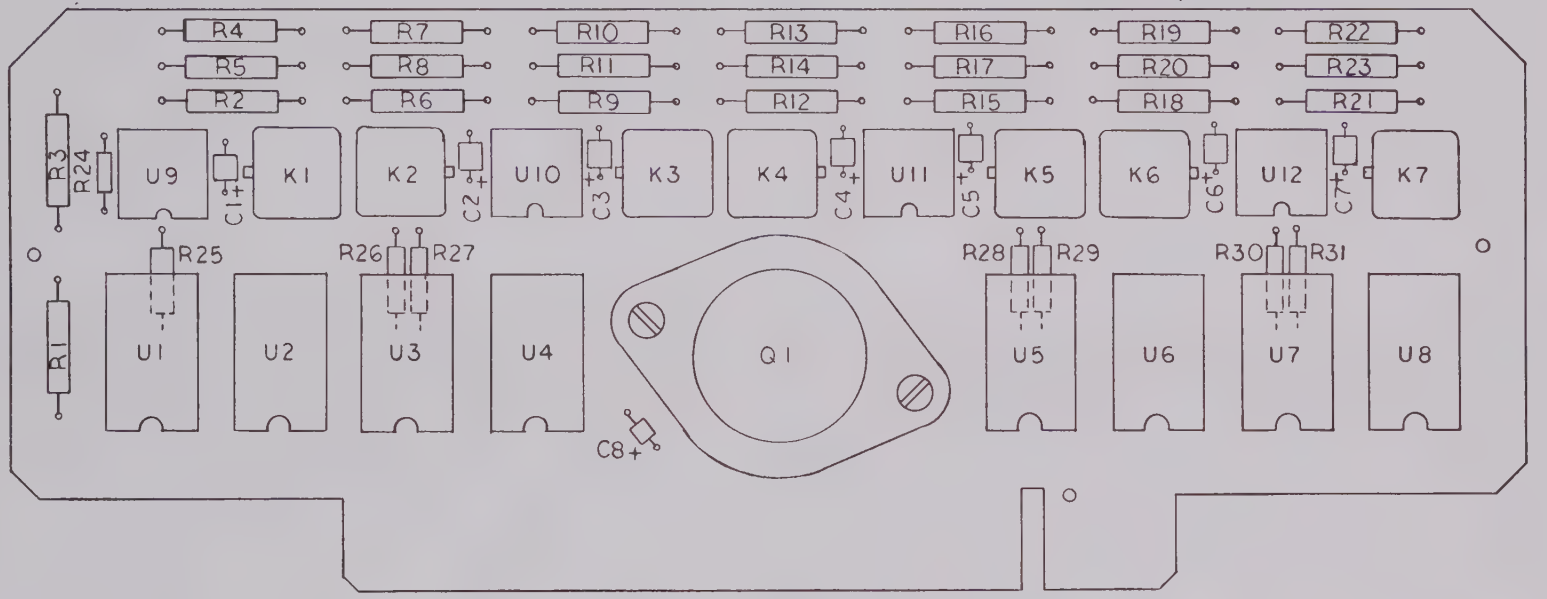
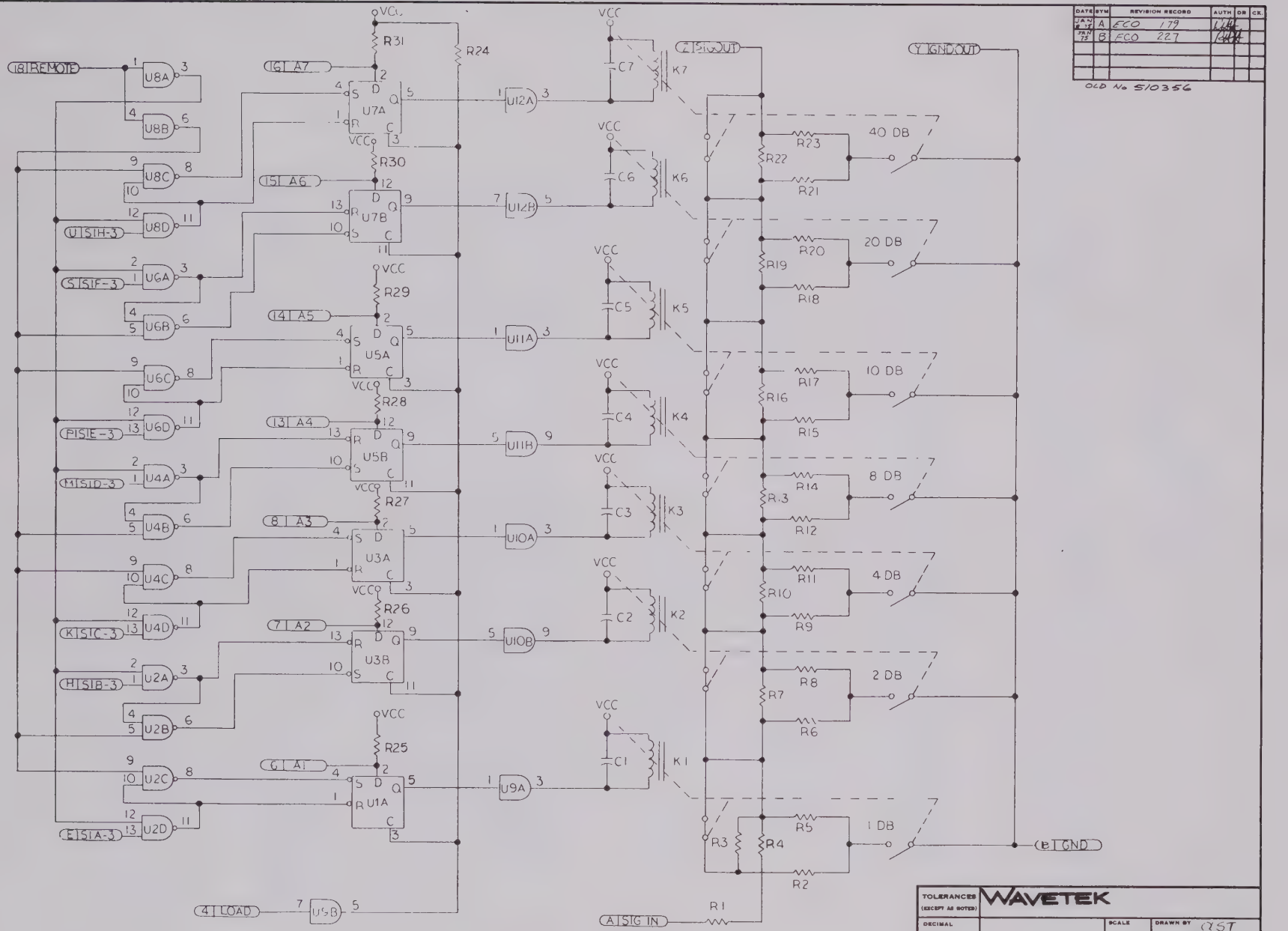


FIGURE 5.9.1

SHEET 1 OF 2

TOLERANCES (EXCEPT AS NOTED)	WAVETEK		
DECIMAL ±		SCALE	DRAWN BY AST
			APPROVED BY
FRACTIONAL ±	TITLE ATTENUATOR ASSEMBLY : REMOTE		
ANGULAR ±	DATE 12-29-71	DRAWING NUMBER 02-004-3077	REV C

K+E ALBANENE ® 10 5400
ENGINEERS' STANDARD PAPER



DATE	SYM	REVISION RECORD	AUTH	DR	CR
JAN 6 73	A	ECO 179			
FEB 73	B	ECO 227			

OLD No 510356

FIGURE 5.9.2

TOLERANCES (EXCEPT AS NOTED)	WAVETEK		
DECIMAL XXX 010 XX 02		SCALE	DRAWN BY GST
			APPROVED BY
FRACTIONAL ± 1/64	TITLE ATTENUATOR ASSEMBLY: REMOTE		
ANGULAR ±	DATE 11-16-72	DRAWING NUMBER 03-004-3077	REV B

ADDENDUM
OPTION 37 REV A

Option 37 provides for the following changes for a Rockland Systems Model 5110 Frequency Synthesizer.

I GROUND STUD

A 1/4-28 MS 2508-4 stud has been installed on the rear panel for connection to system ground. The stud is Rockland Systems P/N 389.8005.

II RACK EARS

The rack ear handles have been changed to a 3.47 inch high unit with finger holes.

III PROGRAMMING CONNECTOR

The program connector on the rear panel has several changes. The changes are as shown in the program line chart.

IV CLOCK INPUT

Option 37 contains an Option 36 printed circuit board which allows the 5110 to be externally clocked by a 1, 5, or 10MHz signal. For the unit to operate correctly, a jumper must be installed in the 1, 5, or 10MHz jumper position. The jumper used is determined by the input clock reference frequency. The input circuit board is located under the top cover and contains the jumpers for setting the unit to the input clock reference frequency.

V OUTPUT LEVEL

The output level of the 5110 has been changed from 10 volts peak to peak to 1 volt RMS with this option. The 1 volt RMS is based on a 50 ohm load.

VI OUTPUT BNC CONNECTOR ON THE FRONT PANEL

A parallel BNC output has been provided on the front panel. It is parallel to the output BNC connector located on the rear panel.

4/14/78
Revised: 8/23/78
Revised: 12/8/78
Revised: 5/14/79

ADDENDUM
5110 OPTION 37 REV B

Option 37 provides for the following changes for a Rockland Systems Model 5110 Frequency Synthesizer.

I GROUND STUD

A 1/4-28 MS 25080-4 stud has been installed on the rear panel for connection to system ground. The stud is Rockland Systems P/N 389.8005.

II RACK EARS

The rack ear handles have been changed to a 3.47 inch high unit with finger holes.

III PROGRAMMING CONNECTOR

The program connector on the rear panel has several changes. The changes are as shown in the program line chart.

IV CLOCK INPUT

Option 37 contains a modified Option 39 printed circuit board which allows the 5110 to be externally clocked by a 1, 5, or 10MHz signal. For the unit to operate correctly, a jumper must be installed in the 1, 5, or 10MHz jumper position. The jumper used is determined by the input clock reference frequency. The input circuit board is located under the top cover and contains the jumpers for setting the unit to the input clock reference frequency. For additional information refer to Pages 1 and 2 of the Option 39 addendum (attached).

V OUTPUT LEVEL

The output level of the 5110 has been changed from 10 volts peak to peak to 1 volt peak to peak with this option. The 1 volt peak to peak is based on a 50 ohm load.

VI OUTPUT BNC CONNECTOR ON THE FRONT PANEL

A parallel BNC output has been provided on the front panel. It is parallel to the output BNC connector located on the rear panel. The coaxial connection between the two output BNC's is rigid coaxial cable.

5110 OPTION 37 REV B

ADDENDUM ATTACHMENT

(HARRIS CORPORATION ONLY)

VII FREQUENCY CONTROL

Reference: Prime Item Product Function Specification
for
Programmable Frequency Synthesizer
18 November 1977

Code Identification No: 91417
Harris ESD 11096 Page 3
Rev C
Paragraph 3.2.1.1.1

Due to this Control Specification the Binary-Word Mode is to be the mode for operation. Therefore the operation of the BCD Mode will not require testing or calibration.

VIII EXTERNAL REFERENCE

Same as basic modified unit. Refer to sections 2.3, 2.3.1 and 2.3.2 of the 5110 Operating Manual.

IX REFERENCE OUTPUT

The Reference Output jack (A5J1) has been deleted from the rear panel. The signal normally brought to this connector has been transferred to the rear panel programming connector pins 1 and 2. The description and derivation of this signal is described in Section 2.4 of the 5110 Operating Manual.

OPTION -38 MANUAL ADDENDA

FOR

MODEL 5110 FREQUENCY SYNTHESIZER

REV A: May 11, 1978

The Model 5110 must be supplied with an 8MHz oscillator reference. A divider circuit has been added to allow for a more versatile operation of the synthesizer. There are two modes that are available:

a) To use the internal 8MHz crystal reference oscillator, place the input reference selector jumper (See Fig. 5.1 of the manual) in the INT position. The Model 5110 can be phase - locked to a 1MHz, 5MHz, or 10MHz external reference oscillator. The position of the jumper on the divider board (located directly in front of the fan) should correspond to the frequency of the external reference oscillator that is supplied at the REF IN BNC jack on the rear panel. The circuit divides the signal at the REF IN BNC by the appropriate amount (as determined by the position of the jumper) to result in a 1MHz reference signal. The pull-in range of this 1MHz signal is ±2Hz.

b) With the input reference selector jumper on the motherboard in the EXT position, (See Fig. 5-1) an external oscillator can be used directly as the reference oscillator, bypassing the internal 8MHz oscillator. The three position jumper on the divider board must be in the "1MHz" position. The frequency limits are 1MHz to 8.1MHz. The deviation of the output signal frequency is directly proportional to the deviation of the external clock from 8MHz. Operation at frequencies below 8MHz results in a lower sampling rate; the internal low pass filter which removes sampling components from the output signal is designed for an 8MHz sampling rate and becomes ineffective as the rate is lowered. To maintain full harmonic and spurious distortion specifications, an ex-

ternal low pass filter is required to eliminate these components.

NOTE

The reference input for either a) or b) above must satisfy the following requirements:

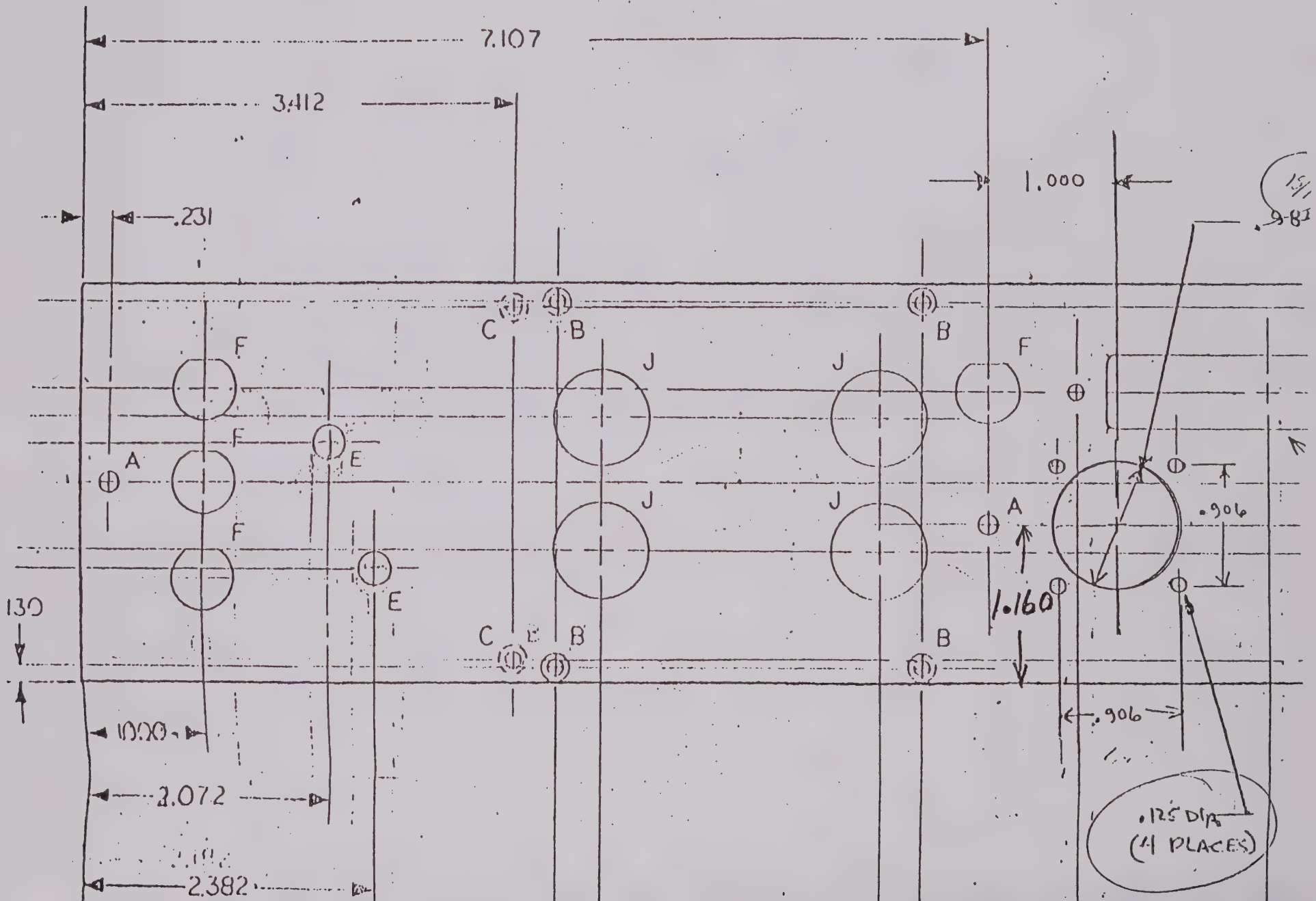
Waveform : Arbitrary; for pulse waveform, 10-90% duty cycle.

Voltage : 200mV P-P to 10 volts P-P

Drive : Input impedence is approximately 200 ohms, AC coupled. May be driven by standard TTL gate.

Manual Changes:

Page	
iii	accepts 1MHz, 5MHz, 10MHz external reference to phase lock the internal crystal.
1-3	See above discussion for phase locking the synthesizer to external crystal reference.
2-1, 2-2	Blank front panel with rear panel cables for power and power indicator.
2-3, 2-4, 2-5	See above discussion for circuit used in phase locking the synthesizer to external crystal reference.
4-3	Delete power switch.
5-3	Delete power switch, power lamp and A4J1 BNC. 2 wires for AC power switching and 2 wires to power lamp are run to the rear panel.
5-11	See drawings and parts list (004-3037).
5-16	Change R22 to R: fxd met flm 249 ohm ± 1% 1/8 W 110-2490 Change R23 to R: fxd met flm 340 ohm ± 1% 1/8 W 110-3400
5-17	Change R22 to 249 ohms and R23 to 340 ohms.
	Delete A4J1 output and associated wiring.
5-18, 5-19	Delete switch A4S3.


7.107
3.412
.231
1.000
.906
1.160
.906
.125 DIA
(4 PLACES)
130
1.000
3.072
2.382
A
B
C
E
F
J

ADDENDA FOR MODEL 5110
MODIFIED FOR
100 μHz FREQUENCY RESOLUTION
OPTION 30

Issued: 8/21/75

Revised: 7/26/78

ADDENDA FOR MODEL 5110
MODIFIED FOR
100 μHz FREQUENCY RESOLUTION
OPTION 30

This document describes the changes to the Model 5110 Frequency Synthesizer Manual caused by the 100 μHz resolution feature.

General

In the programming mode (REMOTE), the frequency resolution is changed from 1 mHz to 100 μHz throughout the frequency range.

Remote Operation

An additional four programming lines are brought to the rear panel via a Cannon DEC-9S connector. Pin assignments are as follows:

Pin	Function	Name
1	100 μHz	M0
2	200 μHz	M1
3	400 μHz	M2
4	800 μHz	M3

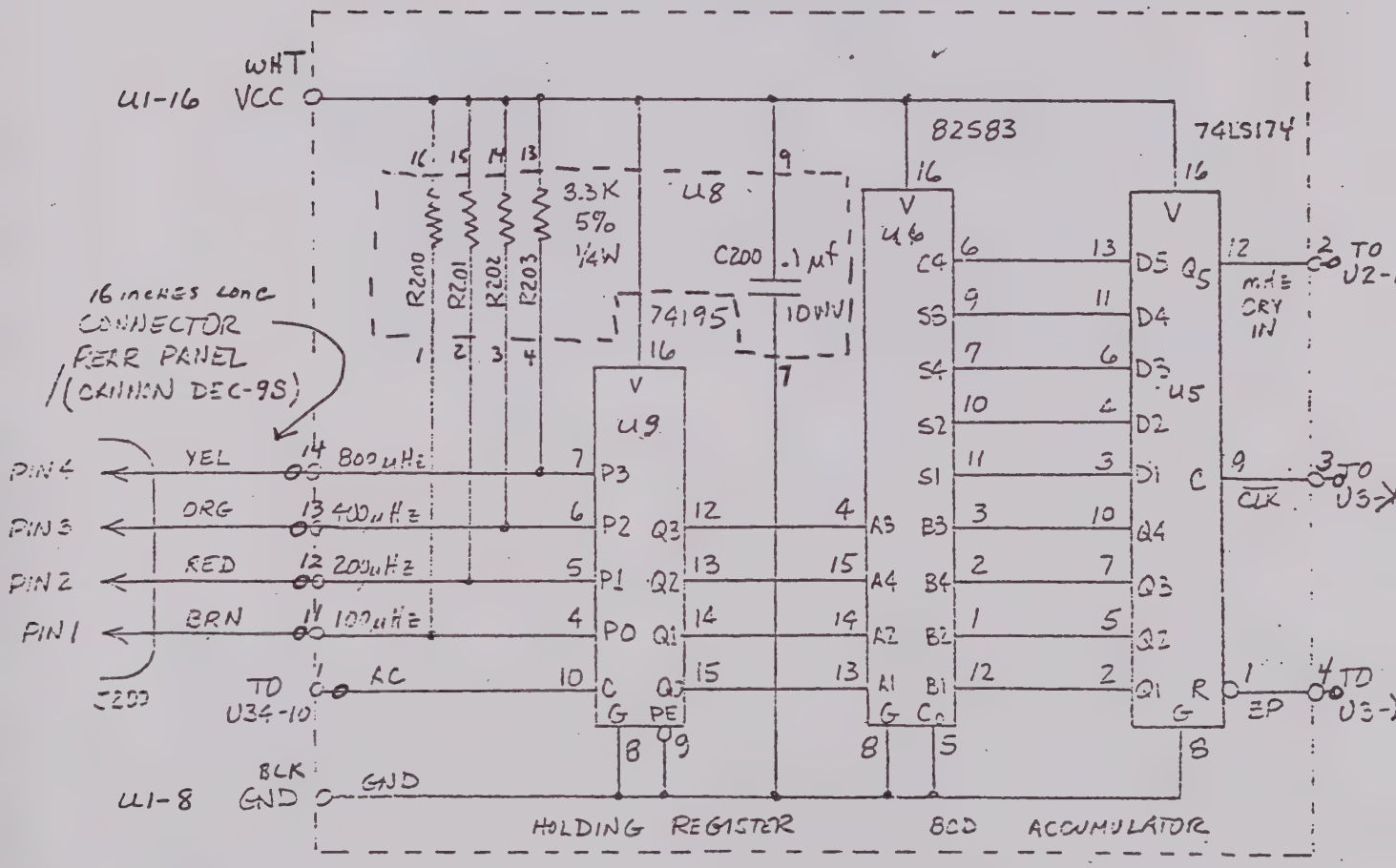
These four lines form a BCD code for 100 μHz resolution. The levels are TTL and input loading is 2 standard TTL loads. Logic is high active, and any BCD value between 0 μHz and 900 μHz is valid. When the instrument is operating in the WORD mode, the data on these lines must be held valid as shown in Figure 2.5 of the manual. When in the BYTE mode, these lines must be held valid during the time shown for the first of four load cycles as shown in Figure 2.5. The weighting of these lines is the same for BCD and BINARY modes.

PARTS LIST

Ref. Desig.	Qty.	Description	Part No.
U9	1	U: 4-Bit Ser/Par Shift Reg (74195)	122-0106
U6	1	U: BCD Adder (82S83)	124-8283
U5	1	U: Hex D-type FF (74LS174)	125-0109
R200	1	R: Fxd comp 3.3K-ohm, 1/4W, 5%	116-2331
R201	1	R: Fxd comp 3.3K-ohm, 1/4W, 5%	116-2331
R202	1	R: Fxd comp 3.3K-ohm, 1/4W, 5%	116-2331
R203	1	R: Fxd comp 3.3K-ohm, 1/4W, 5%	116-2331
C200	1	C: Fxd cer disc .1 µf, 10WV	100-4100
J200	1	Cannon DEC-9S Socket Connector	
D200	1	Cannon DEC-9P Plug Connector	
	1	Header	352-1602
	1	PC Board	320-3099
	4	16 Pin WW IC Socket	353-1602
	2	M SCR: ST CD SL 6-32 x 1/4 PH	380-6042
	16	Conn: Term Pin WW .025 Gold Plt	354-0003
		16" Wire: #24 AWG STR Black	378-1704
		16" Wire: #24 AWG STR Brown	378-1714
		16" Wire: #24 AWG STR Red	378-1724
		16" Wire: #24 AWG STR Orange	378-1734
		16" Wire: #24 AWG STR Yellow	378-1744
		16" Wire: #24 AWG STR White	378-1794

ISOLATE U2-13 From Ground on MAIN board.

03-004-3090



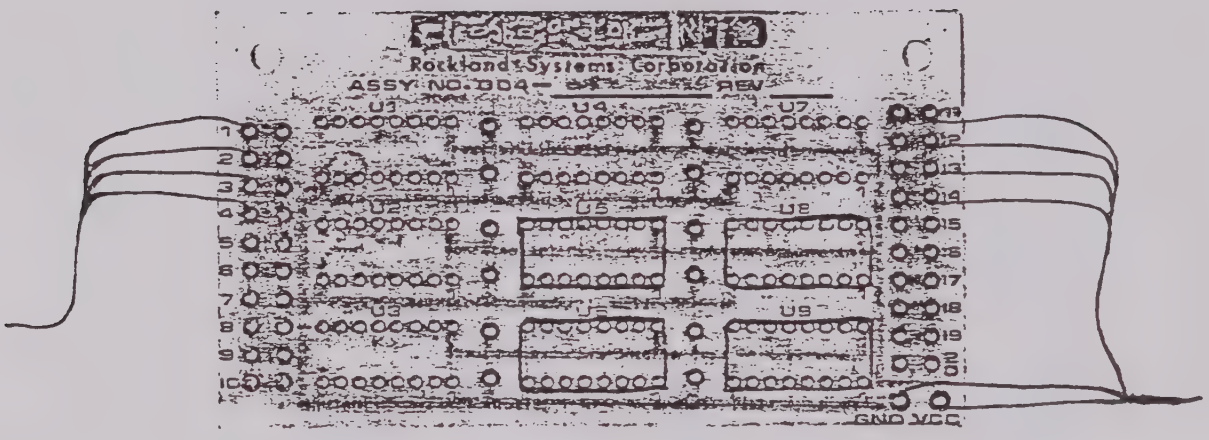
Pfatt 8/21/75

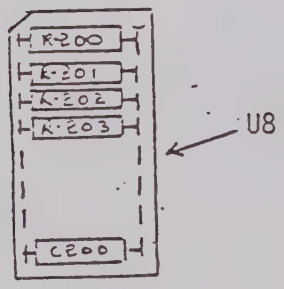
R Hosking 8/21/75

MODEL 5100 100 µHz FREQUENCY
RESOLUTION EXTENDER

02-004-3090

5100 Left Side, Top





NOTE: Cut WW Pins to 3/8" Max.

MODEL 5100 or 5110 ADDENDA

OPTION 20

General: Option 20 provides a TTL compatable square wave signal connected to a rear panel BNC jack labeled TTL OUTPUT. The TTL compatable square wave output maintains the same frequency range and resolution applied to the standard 5100/5110 outputs. The TTL OUTPUT BNC jack replaces the auxiliary VAR OUTPUT jack on the 5100 rear panel.

Operation and Circuit Description:

The circuitry required to generate the square wave output is contained on the Option 20 circuit board assembly (RSC P/N 004-3098), which is attached to the inside, center portion of the 5100/5110 left side panel.

Refer to the following documents for additional information:

1. Modification of 51xx for Option 20 TTL output. RSC P/N 02-002-3050.
2. Schematic, Option 20 TTL Output. RSC P/N 03-004-3098.
3. Assembly, Option 20 TTL Output. RSC P/N 02-004-3098.

The TTL output circuitry consists of an LM361 (high speed differential comparator) and a DM8830 (line driver, single-ended configuration), used with a shorting plug to select either the NON-INVERT or the INVERT output.

The following steps are required to properly set the shorting plug. Determined the TTL output phase requirement, with respect to the 5100/5110 standard output. If the complement wave form is desired, remove (2) screws securing the top cover to the rear panel. Slide the top cover toward the rear panel until the Option 20 board assembly is fully exposed. Set the shorting plug to the required position.

NOTE: The shorting plug must be set between Output and NON-INV or Output and INV to provide a TTL output at the rear panel TTL OUTPUT BNC jack.

After the shorting plug has been properly set, replace the top cover and secure the (2) rear panel screws.

The following is a partial list of the DM8830 electrical characteristics applicable to the Option 20:

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" output voltage	I out = -0.8ma	2.4			V
" "1" " "	I out = 40ma	1.8	3.3		V
" "0" " "	I out = +32ma		0.2	0.4	V
" "0" " "	I out = +40ma		0.22	0.5	V

5100 Manual Changes:

Page i Output Signals. Change second sentence of Variable Output description to read front panel BNC jack.

Documentation: Delete all reference to the rear panel VAR Output jack.

10/16/78
6-23-83 REV: B

WAVETEK, INC.

MODEL 5100 or 5110 ADDENDA

OPTION 20

General: Option 20 provides a TTL compatable square wave signal connected to a rear panel BNC jack labeled TTL OUTPUT. The TTL compatable square wave output maintains the same frequency range and resolution applied to the standard 5100/5110 outputs. The TTL OUTPUT BNC jack replaces the auxiliary VAR OUTPUT jack on the 5100 rear panel.

Operation and Circuit Description:

The circuitry required to generate the square wave output is contained on the Option 20 circuit board assembly (RSC P/N 004-3098), which is attached to the inside, center portion of the 5100/5110 left side panel.

Refer to the following documents for additional information:

1. Modification of 51xx for Option 20 TTL output. RSC P/N 02-002-3050.
2. Schematic, Option 20 TTL Output. RSC P/N 03-004-3098.
3. Assembly, Option 20 TTL Output. RSC P/N 02-004-3098.

The TTL output circuitry consists of an LM361 (high speed differential comparator) and a DM8830 (line driver, single-ended configuration), used with a shorting plug to select either the NON-INVERT or the INVERT output.

The following steps are required to properly set the shorting plug. Determined the TTL output phase requirement, with respect to the 5100/5110 standard output. If the complement wave form is desired, remove (2) screws securing the top cover to the rear panel. Slide the top cover toward the rear panel until the Option 20 board assembly is fully exposed. Set the shorting plug to the required position.

NOTE: The shorting plug must be set between Output and NON-INV or Output and INV to provide a TTL output at the rear panel TTL OUTPUT BNC jack.

After the shorting plug has been properly set, replace the top cover and secure the (2) rear panel screws.

The following is a partial list of the DM8830 electrical characteristics applicable to the Option 20:

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" output voltage	I out = -0.8ma	2.4			V
" "1" " "	I out = 40ma	1.8	3.3		V
" "0" " "	I out = +32ma		0.2	0.4	V
" "0" " "	I out = +40ma		0.22	0.5	V

5100 Manual Changes:

Page i Output Signals. Change second sentence of Variable Output description to read front panel BNC jack.

Documentation: Delete all reference to the rear panel VAR Output jack.

NOTE: When Option -20 is used with a Model 5100-13 and the desired output frequency is above 2MHz, the variable output level must be set to maximum to insure a square wave output.

MODEL 5100 or 5110 ADDENDUM

OPTION 39

General: Option 39 consists of a circuit that can be included in the Rockland Systems Corporation Model 5100 or 5110 Frequency Synthesizers. The purpose of this option is to expand the 5100/5110 Phase Locking capablility from accepting a 1MHz external clock reference only, to accepting either a 1MHz, 5MHz or 10MHz external clock reference. The circuitry required to accomplish the functions of Option 39 is contained on a printed circuit board assembly, RSC P/N 02-004-3036, and a schematic reference diagram 03-004-3036.

Circuit Description:

The circuitry shown on schematic diagram 03-004-3036 contains two seperate functions. The first section, consisting of all components between the input to C3 and the output of Q2 (collector) offers an A.C. coupled high input impedance to the input signal which is amplified and shaped to a TTL compatible waveform. The second section, consisting of IC U1 (7490) and an input clock selector jumper, present the required 1MHz signal to the CLOCK OUT line. Refer to the following table:

INPUT	U1-Pin 1	U1-Pins 11, 14	U1-Pin 12	JUMPER POSITION	OUTPUT
1MHz	1MHz	200KHz	100KHz	U1-Pin 1 to Clock Out	1MHz
5MHz	5MHz	1MHz	500KHz	U1-Pin 14 to Clock Out	1MHz
10MHz	10MHz	2MHz	1MHz	U1-Pin 12 to Clock Out	1MHz

ONE OF THE REFERENCE SIGNALS MUST BE CONNECTED TO THE CLOCK OUT LINE BY SELECTOR JUMPER OR THE CIRCUIT WILL NOT WORK.

Initial Set Up of Option 39:

The steps required for the proper operation of Option 39 are as follows:

Remove two (2) screws securing the top cover to the rear panel. Slide the top cover toward the rear panel until the Option 39 board assembly is fully exposed. (The 02-004-3036 board assembly is attached to the inside, rear center portion of the 5100/5110.)

Determine the EXTERNAL REFERENCE frequency to be connected to the Reference Input BNC and set the Option 39 selector selector jumper accordingly.

i.e. 1MHz external standard input: set selector jumper between OUT and 1MHz.

5MHz external standard input: set selector jumper between OUT and 5MHz.

10MHz external standard input: set selector jumper between OUT and 10MHz.

At this point the INT/EXT selector on the 5100/5110 motherboard must also be set to INT. Refer to figure 5.1 of the 5100 or 5110 manual. (Note: Option 39 must be ordered with either Option 01 (High Stability Xtal) or Option 06 (Standard Xtal).) After verifying both selector jumpers reinsert and secure the top cover.

Manual Changes:

ALL reference to External 1MHz reference input signal should be changed to External 1, 5 or 10MHz reference input.

ALL references to the pull-in range of the phase-locked loop apply to the signal at the CLOCK OUT line.

WAVETEK

February 16, 1981

MANUAL ADDENDA

MODEL 5110-12

FREQUENCY SYNTHESIZER

Manual Part Number 800-0312

1. On page 5-2, CHANGE description and Part No. as follows:

REF. DES.	DESCRIPTION	PART NO.
C35	C: fxd mon 0.1 ufd + 80 - 20% 10V	100-4102
R5	R: fxd comp 560 ohm 5% 1/4W	116-1561
R20	R: fxd comp 10K 5% 1/4W	116-3101
DAC1	Converter: D/A 10 bit	004-3056

On page 5-2, ADD as follows:

R50	R: fxd metflm 453 ohm 1% 1/8W	110-4530
R59	R: fxd comp 470 ohm 5% 1/4W	116-1471
R61	R: fxd comp 47K 5% 1/4W	116-3471

On page 5-2 DELETE as follows:

R56	R: fxd comp 100 ohm 5% 1/4W	116-1101
R57	R: fxd comp 220 ohm 5% 1/4W	116-1221
R58	R: fxd comp 220 ohm 5% 1/4W	116-1221

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2. On page 5-3, CHANGE description and Part No. as follows:

U85	U: dual D type flip flop	122-7474
U100	U: dual D type flip flop	124-7474
U101	U: dual D type flip flop	124-7474
U102	U: dual D type flip flop	124-7474
U103	U: dual D type flip flop	124-7474
U104	U: dual D type flip flop	124-7474
U105	U: dual D type flip flop	124-7474

3. On page 5-4 CHANGE description and Part No. as follows:

REF. DES.	DESCRIPTION	PART NO.
C29	C: fxd elect 47 MFD 63 WVDC ±20%	109-6470
C31	C: fxd elect 47 MFD 63 WVDC ±20%	109-6470
C32	C: fxd mica 820 pf ±1% 500WVDC	101-1820
L1	Inductor: fxd 4.7 UHY ±10%	150-9470
Q10	Transistor: silicon NPN	134-2222
Q14	Transistor: silicon PNP	136-2905
R22	R: fxd met film 432 ohm ±1% 1/10W	110-4321
R30	R: fxd met film 1K ±1% 1/10W	111-1001
R60	R: fxd met film 49.9 ohm 1% 1/8W	119-4990

On page 5-4 ADD description and Part No. as follows:

CR14	Diode: sil gen. purp.70 PIV	132-0457

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4. On page 5-5, CHANGE description and Part No. as follows:

C4	C: Fxd, Cer, 0.1 MFD, +80 - 20%, 10V	100-4101
C5	C: Fxd, Cer, 0.1 MFD, +80 - 20%, 10V	100-4101

On page 5-5 ADD description and Part No. as follows:

C96	C: Fxd, Tant. Elect, 0.1 MFD ±20%, 35WVDC	109-4100

ADDENDUM FOR MODEL 5110-06-20

Mod 132

General: The REF OUT Ftn is deleted. The internal load line is removed from 50 pin conn. and connected to the REF OUT BNC.

Instructions: Remove wire from A5J1 pin 12 to U31 pin 4. Remove Coax cable from REF OUT BNC to main board (load line).

Add twisted pair from U31-4 and adjacent U20 gnd to REF OUT BNC on rear panel.

Change marking of rear panel REF OUT to read STROBE INPUT TTL. (The STROBE now replaces the load line). Refer to Remote Programming Section of the Manual.

pc

Customer: Boeing Aerospace

MANUAL ADDENDA

MODEL 5110

FREQUENCY SYNTHESIZER

Manual Part Number 800.0311

PURPOSE:

In order to improve long term component reliability, the following change has been implemented.

DESCRIPTION:

Heat Sink mounted onto Q12 of 10 Bit DAC-1 for more efficient heat dissipation.

MANUAL REFERENCE DWG. NO.:

02-004-3110

REFERENCE DWG NO. (ATTACHED):

02-004-3056 Sheets 1 and 2

ADD:

Item	P/N	QTY	Description	Remarks
33	367-0413	1	Heat Sink	Installed on Q12
	TYPE: AVVID ENG. INC. - Part No. 3224B or equivalent			

NOTE:

Insert REFERENCE DRAWINGS and ADDENDA to manual.

ADDENDUM TO MODEL 5100 MANUAL FOR SPECIAL DIVIDE BY 10 FEATURE

Addendum to Model 5100 Manual
For Special Divide by 10 Feature

The Model 5100 Frequency Synthesizer has been modified to accept a 10 MHZ input signal, and phase lock it to the internal oscillator of the Model 5100. The 1 Vp-p fixed output level on the rear panel (FXD OUT) has been sacrificed, although it is still available on the front panel jack.

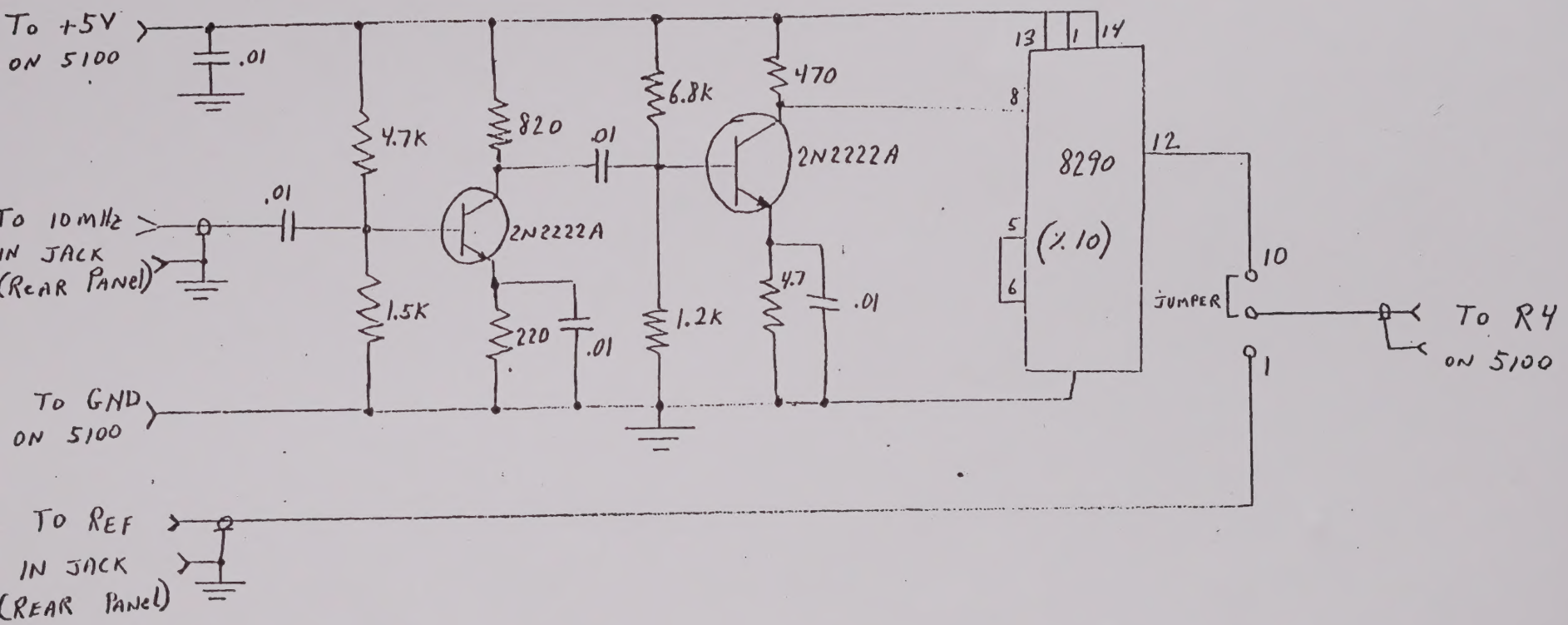
The 1 MHZ, or 8 MHZ, reference capability is still available via selection of an internal jumper.

Operation:

1. To phase lock the Model 5100 Frequency Synthesizer to an external 10 MHZ reference, the 10 MHZ input must be connected to the 10 MHZ IN jack on the rear panel (formerly FXD OUT).
   The Input Reference Selector jumper on the Model 5100 motherboard must be in the INT position.
   An additional circuit has been mounted on the side panel of the Model 5100. The jumper on this board must be in the 10 position. The 10 MHZ input can be TTL, or a sine wave input with amplitude from 10 mVrms to 1 Vrms.

2. To phase lock the Model 5100 Frequency Synthesizer to 1 MHZ, or operate the Model 5100 from an external 8 MHZ standard, the jumper on the additional board mounted on the side panel must be in the 1 position. The Input Reference Selector jumper on the Model 5100 motherboard must be set to the appropriate position (that is, INT for 1 MHZ and EXT for 8 MHZ). The input 1 MHZ or 8 MHZ reference is still connected via the REF IN jack on the rear panel of the Model 5100. The amplitude requirements are as per the Model 5100 manual specifications.

Note: The pull-in range of the phase-locked loop is ± 2 HZ at 1 MHZ or ± 20 HZ at 10 MHZ.



SCHEMATIC FOR SPECIAL
TO ACCEPT 10 MHz INPUT

MP MASTER
MA35650

93281